BetterV: Controlled Verilog Generation with Discriminative Guidance

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Abstract

We propose a framework, BetterV, for controlled Verilog generation. BetterV utilizes a generative discriminator to guide the Large Language Models (LLMs) to generate Verilog code that aligns with a pre-trained C model. BetterV outperforms existing tools like CodeQwen in terms of functional correctness and optimization. BetterV’s performance can be further improved by incorporating more datasets and evaluation benchmarks.

1. Background

LLMs based Verilog Generation

Given the natural language descriptions as input, the large language models (LLMs) try to output the Verilog code. The generated Verilog is expected to be syntactically and functionally correct.

2. Methodology

2.1 Code Knowledge Transfer

We design a novel instruction-tuning process to align the generated Verilog code with the pre-trained C model. This ensures that the generated Verilog code maintains the functional correctness of the C model.

2.2 Discriminative Guidance

We utilize a generative discriminator to guide the LLMs to generate Verilog code that aligns with the pre-trained C model. This helps in improving the optimization of the generated Verilog code.

3. Experiments

BetterV outperforms existing tools like CodeQwen in terms of functional correctness and optimization. BetterV’s performance can be further improved by incorporating more datasets and evaluation benchmarks.

4. Conclusion

BetterV provides a controlled way to generate Verilog code that aligns with the requirements set by the C model. This helps in improving the optimization of the generated Verilog code.

References

