Performance-Driven Analog Layout Automation: Current Status and Future Directions

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Introduction
Digital vs Analog Circuits

Data
- Digital
  - Boolean
  - "1"
  - "0"
- Analog
  - Real
  - (( ● )))

Reliability
- Robust

Design
- Automated
- Sensitive
- Manual
• Heavily manual, iterative process involving multiple steps to achieve performance, power and area closure.

• More challenging with performance closure: complicated circuit performance metrics, sensitive signal integrity and performance trade-offs

• **Open question**: how can we optimize *performance* in automated layout generation?
Analog IC automation typical flow:

- Today we will focus on the back-end side
Develop optimization-based PNR algorithms for analog layouts

Pros

• Automatic optimization
• Low human efforts

Cons

• What is the optimization problem?
• How to consider performance?

The design flow of analog circuits.
Related Work
Analog circuit placement and routing are critical to optimal performance, but obtaining a decent circuit layout requires significant time and expertise:

- Unlike digital circuits, analog circuits are sensitive to layout parasitics and coupling, which can complicate the relationship between performance and layout.
- There lacks a practical way to produce generalized performance models for layout implementation\(^1\).

Let’s first take a look on existing attempts to consider performance in PNR

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The existing analog layout placement methods are mainly focused on optimizing proxy objectives for performance:

- **Symmetry and common centroid**\(^2\);

For example, using common centroid placement to reduce parasitic mismatch. **Question:** Is symmetry good enough for the performance?

2-D symmetry (b) does not include placement (a) which also satisfies the common centroid constraint.

• **Current path and signal flow**

Zhu et al.\(^4\) propose to consider the critical signal paths in automatic AMS placement. **Question**: enough for general circuits?

The analog router cannot adopt specialized layout strategies for specific circuit classes like human layout experts, so proxy heuristic method is honored in performance-driven analog routing.

- **Symmetry** has been widely adopted as an essential component of the analog routing problem.

Example: different levels of geometrical matching constraints.

(a) Symmetric constraint. (b) Common-centroid constraint. (c) Topology-matching constraint. (d) Length-matching constraint.

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Other works optimize power routing\(^7\) and propose shielding critical nets\(^8\).

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• **Linear approximation model**

Lampaert et al.\(^9\) uses performance degradation term. Characterising performance degradation \(\Delta P_j\) using the precalculated sensitivity information:

\[
\Delta P_j = \sum_{k=1}^{m} \left( S_{C_p,k}^j C_p,k + \sum_{i=1}^{n_k} S_{R_p,ki}^j R_p,ki \right) 
\]

(1)

**Issues**: sensitivity computation scalability and accuracy.

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Machine learning methods provide a **direct** way to model the post-layout analog performance\(^\text{10}\)

- Automatically generate layout data and extract effective placement features based on functionality;
- Utilize 3D Convolutional Neural Networks (CNNs) as the performance predictor, incorporating coordinate channels.

There are also attempts to apply learning models to analog placement:

- Utilize the GNN performance model as a predictor.
- Employ the performance predictor to guide the simulated annealing process.

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Case Study
The performance modeling cycle can be divided into three stages:

- **Data Acquisition**: The data acquisition stage includes PNR and parasitic parameter extraction (PEX) and post-layout performance simulation (Post-Sim).

- **Model Training**: The model training stage mainly includes the Training time for performance models.

- **Performance-aware PNR Inference**: The performance-aware PNR inference includes the model Inference time and a single **augmented PNR** process.
Case 1: Analog Performance Modeling Lifecycle

Profiling lifecycle for building a performance model on Operational Transconductance Amplifier (OTA) layout design using MAGICAL.

(a) The runtime breakdown of different methods on OTA1 benchmarks.
Observations from Case 1

We can draw two important observations from Case 1:

1. The **Data Collection** occupies **most** of the modeling lifecycle, which accounts for 92.89%.

2. The time required to obtain **inputs** $\ll$ the time required to obtain **labels**. *(The PEX and Post-Sim time is roughly equivalent to 3-4 PNR iterations.)*
How to shorten the performance modeling lifecycle effectively?

Reduce the time spent on data acquisition, especially PEX and Post-Sim.

There are several promising solutions:

- From advancements in hardware-accelerated EDA workflows\textsuperscript{12}, we can see that parallelizing PEX and Post-Sim is an effective solution.

- Considering the cost of acquiring data inputs and labels, selecting representative samples through active learning\textsuperscript{13} may also be an economically efficient approach.

- ...


In the case shown in the Table 1, we quantitatively discuss the issue of performance model transferability on OTA designs.

### From Scratch

- A small amount of sampling data for the current design is collected.
- We then model the prediction as a binary classification problem to achieve accurate predictions\(^\text{14}\).

### Transfer

- The pre-trained model obtained from other designs is leveraged.
- We can obtain a relatively accurate model with a few samples through fine-tuning, which requires less time.

We mainly consider two scenarios of Transfer:

### Transfer between the same topology
- We first train a performance model on OTA3. **OTA3 has the same topology and different sizing configurations as OTA1.**
- We then test the accuracy of model predictions on OTA1.

### Transfer between different topologies
- We first train a performance model on OTA3. **OTA3 has different topologies from OTA2.**
- We then test the accuracy of model predictions on OTA2.
From these data results, we can identify two important findings:

- The transferability of the models varies under different scenarios and metrics, with the accuracy reduction ranging from 3% to 22%.
- Transfer between different sizing configurations is often easier than transfer between different topologies.
From a Generalization Perspective

• We consider how to improve transfer training by obtaining effective pretraining weights using methods like meta-learning\textsuperscript{15}.

From a Detection Perspective

• We consider different distributions to determine when the transfer is safe.
• Current research on out-of-distribution (OOD) detection\textsuperscript{16} provides technical support for identifying when the model is effective.


\textsuperscript{16}Qitian Wu et al. (2022). “Energy-based Out-of-Distribution Detection for Graph Neural Networks”. In: Proc. ICLR.
In this case, we aim to demonstrate the importance of multi-objective optimization by comparing the placements obtained through weighted-based Bayesian optimization (BO) and multi-objective optimization Bayesian optimization (MOBO)\(^\text{17}\) in four OTA benchmarks.

**Weighted Method**

- It is common practice to use a user-defined figure-of-merit (FOM) representation, a weighted sum of post-layout simulation metrics.

**Multi-objective Optimization**

- One alternative objective is to find solutions not dominated by others, known as Parcel optimal solutions.
- The problem of finding Pareto optimal solutions given multiple criteria is called multi-objective optimization.

As shown in Figure 12, the MOBO method outperforms Weighted-BO in terms of the number of top-1 metrics achieved for the obtained layout.

The number of top-1 metrics for different methods.

- MOBO achieves top-1 performance in almost all metrics in Offset Voltage, CMRR, BandWidth, and DC Gain.
- For all designs, MOBO outperforms the Weighted-BO for 3 to 5 metrics.
The results corroborate that the multi-objective optimization method moves the layout solution toward the Pareto frontier.

Recent advancements have been witnessed in the field of multi-objective optimization, especially for gradient-based strategies\textsuperscript{18}.

It is imperative to carefully consider how these advancements in the field of multi-objective optimization can be applied to enhance performance-driven analog layout automation.

Perspectives and Future Directions
Efficient Data Acquisition

- Data collection bottleneck in building performance models;
- Active learning for selecting representative samples\textsuperscript{19};
- Smart layout selection for an efficient training process;
- Accelerating simulation for more training data\textsuperscript{20};


Better Transferability

- Transferring pre-trained models to unseen circuits Managing multimodal input features;
- A general multimodal neural network for performance modeling may benefit the field\(^\text{21}\);
- Adopting a pretraining methodology for data efficiency\(^\text{22}\);


Placement and Routing Representation

• Placement and Routing Representation: An overlooked problem in ML-enabled performance-driven analog physical design is how to represent placement and routing. The work\textsuperscript{23} treats the performance modeling as a black box.

• Bridging Placement and Routing Representation for Optimization: BO-based framework tunes net weights as a proxy to generate different placements in\textsuperscript{24}.

\textsuperscript{23}Yaguang Li, Yishuang Lin, Meghna Madhusudan, Arvind Sharma, Wenbin Xu, Sachin Sapatnekar, et al. (2020). “A Customized Graph Neural Network Model for Guiding Analog IC Placement”. In: Proc. ICCAD.

Multi-objective Optimization

- Complexity of analog circuit performance
- Multiple competing performance metrics
- Efficient and effective multi-objective physical design optimization
THANK YOU!