#### THE CHINESE UNIVERSITY OF HONG KONG Print Course Catalog Details

### Academic Org: Dept of Computer Sci & Engg - Subject: Computer Science

Course: CSCI2510	Course ID: 002577	Eff Date: 2024-07-01	Crse Status: Active	Apprv. Status: Approved	[Course Rev]
Computer Organization 計	算機結構				

This course is designed to provide the basic knowledge of computer organization and assembly language programming. Functions and structures of the basic building blocks: CPU, memory unit and input/output units will be introduced. Assembly language programming is used as a tool to study the internal coding of information, number representation, arithmetic operations and the flow of information within a microcomputer.

## 本科旨在提供計算機結構及匯編語言程序設計的基本知識。介紹基本構件的功能及結構:中央處理器、存儲器及輸入輸出部件。以匯編語言程序設計為工具來研究信息的內部 編碼、數字表示法、算術運算及微計算機中的信息流。

### Grade Descriptor: A

EXCELLENT – exceptionally good performance and far exceeding expectation in all or most of the course learning outcomes; demonstration of superior understanding of the subject matter, the ability to analyze problems and apply extensive knowledge, and skillful use of concepts and materials to derive proper solutions.

#### 有關等級說明的資料,請參閱英文版本。

В

GOOD – good performance in all course learning outcomes and exceeding expectation in some of them; demonstration of good understanding of the subject matter and the ability to use proper concepts and materials to solve most of the problems encountered.

#### 有關等級說明的資料,請參閱英文版本。

С

FAIR – adequate performance and meeting expectation in all course learning outcomes; demonstration of adequate understanding of the subject matter and the ability to solve simple problems.

#### 有關等級說明的資料,請參閱英文版本。

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MARGINAL – performance barely meets the expectation in the essential course learning outcomes; demonstration of partial understanding of the subject matter and the ability to solve simple problems.

## 有關等級說明的資料,請參閱英文版本。

F

FAILURE – performance does not meet the expectation in the essential course learning outcomes; demonstration of serious deficiencies and the need to retake the course.

## 有關等級說明的資料,請參閱英文版本。

Equivalent Offering:	
Units:	3 (Min) / 3 (Max) / 3 (Acad Progress)
Grading Basis:	Graded
Repeat for Credit:	Ν
Multiple Enroll:	Ν
Course Attributes:	

Topics:

	COURSE OUTCOMES
Learning Outcomes:	
	1. Understand the principles of computer architectures including I/O, memory organization and the processor
	2. Be able to write assembly language programs
	3. Be able to select the best I/O scheme (polling, interrupt or DMA) for a given problem
Course Syllabus:	
	This course is designed to provide the basic knowledge of computer organization and assembly language programming.
	Functions and structures of the basic building blocks: CPU, memory unit and input/output units will be introduced. Assembly
	language programming is used as a tool to study the internal coding of information, number representation, arithmetic operations
	and the flow of information within a microcomputer.

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Feedback for Evaluation: 1. Midterm evaluation 2. Questions in labs/tutorials	
Required Readings: 1. Hamacher, Vranesic, Zaky, Computer Organization (5th ed.), McGraw Hill, 2002	
Recommended Readings:	
OFFERINGS	
1. CSCI2510 Acad Organization=CSD; Acad Career=UG	
COMPONENTS	
LEC : Size=30; Final Exam=Y; Contact=3 TUT : Size=30; Final Exam=N; Contact=1	
ENROLMENT REQUIREMENTS	
1. CSCI2510 Enrollment Requirement Group: Not for students who have taken CENG2400 or ELEG3230 or ENGG2020 or ESTR2100 or ESTR2104. Prerequisite: CSCI1120 or 1130 or 1510 or 1520 or 1530 or 1540 or 1550 or ENGG1110 or ESTR1002 or 1100 or MATH2221 or PHYS2061.	r 1102 or
New Enrollment Requirement(s): Pre-requisite = change from "CSCI1110 or 1120 or 1130 or 1510 or 1520 or 1530 or 1540 or ENGG1110 or EST 1100 or 1102 or (MATH2210 and MATH2220) or PHYS2351" to "CSCI1120 or 1130 or 1510 or 1520 or 1530 or 1540 or 1550 or ENGG1110 or ESTR1002 or 1100 or MATH2221or PHYS2061" Exclusion = no change	
Additional Information	

eLearning hrs for blended cls0VTL-Onsite face-to-face hrs0VTL-Online synch. hrs0

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VTL-Online asynch. hrs 0 No. of micro-modules 0 Research components (UG) 0%

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