CU_CURR501
Page 1 of 3

THE CHINESE UNIVERSITY OF HONG KONG
Print Course Catalog Details

May 10, 2023
12:36:40 PM

 Academic Org: Dept of Computer Sci & Engg – Subject: Computer Engineering

Course: CENG3420   **Course ID:** 001784   **Eff Date:** 2022-07-01   **Crse Status: Active**   **Apprv. Status:** Approved   【Course Rev】

Computer Organization and Design 計算機組成與設計

This course introduces the organization and design of modem computer systems. The scope includes instruction set architecture, performance evaluation, design of arithmetic logic units, datapath and control, pipelining, memory hierarchy, interfacing processors and peripherals, and multi-core processors.

本科介紹現代計算機之組成與設計，內容包括指令集、性能評價、運算邏輯單元設計、數據通路及控制、流水線技術、存儲器之分級體系、介面處理機及外圍設備、以及多核處理器。

Grade Descriptor: A

EXCELLENT – exceptionally good performance and far exceeding expectation in all or most of the course learning outcomes; demonstration of superior understanding of the subject matter, the ability to analyze problems and apply extensive knowledge, and skillful use of concepts and materials to derive proper solutions.

有關等級說明的資料，請參閱英文版本。

B

GOOD – good performance in all course learning outcomes and exceeding expectation in some of them; demonstration of good understanding of the subject matter and the ability to use proper concepts and materials to solve most of the problems encountered.

有關等級說明的資料，請參閱英文版本。

C

FAIR – adequate performance and meeting expectation in all course learning outcomes; demonstration of adequate understanding of the subject matter and the ability to solve simple problems.

有關等級說明的資料，請參閱英文版本。

D

MARGINAL – performance barely meets the expectation in the essential course learning outcomes; demonstration of partial understanding of the subject matter and

CU_CURR501
Page 2 of 3

THE CHINESE UNIVERSITY OF HONG KONG
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12:36:40 PM

the ability to solve simple problems.

有關等級說明的資料，請參閱英文版本。

F

FAILURE – performance does not meet the expectation in the essential course learning outcomes; demonstration of serious deficiencies and the need to retake the course.

有關等級說明的資料，請參閱英文版本。

Equivalent Offering:
Units: 3 (Min) / 3 (Max) / 3 (Acad Progress)
Grading Basis: Graded
Repeat for Credit: N
Multiple Enroll: N
Course Attributes:

Topics:

COURSE OUTCOMES

Learning Outcomes:

Student will be able to
1. design pipelined microprocessor using Hardware Description Language;
2. evaluate the performance of computer systems;
3. measure the memory access performance of a processor, and tune cache design parameters to improve performance;
4. translate simple programs from C to machine language.

Course Syllabus:

This course introduces the organization and design of modem computer systems. The scope includes instruction set architecture, performance evaluation, design of arithmetic logic units, datapath and control, pipelining, memory hierarchy, interfacing processors and peripherals, and multi-core processors.

Assessment Type:

Essay test or exam	: 60%
Others	: 40%

CU_CURR501
Page 3 of 3

THE CHINESE UNIVERSITY OF HONG KONG
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May 10, 2023
12:36:40 PM

Feedback for Evaluation:

1. Mid-term evaluation;
2. Office hours;
3. In-class and tutorial questions;

Required Readings:

1. Patterson and Hennessy, Computer Organisation & Design, The Hardware/Software Interface, 3rd edition

Recommended Readings:

OFFERINGS

1. CENG3420   Acad Organization=CSD; Acad Career=UG

COMPONENTS

LEC : Size=30; Final Exam=Y; Contact=3
TUT : Size=30; Final Exam=N; Contact=1

ENROLMENT REQUIREMENTS

1. CENG3420   **Enrollment Requirement Group:**
                     Not for students who have taken CSCI3420.
                     Prerequisite: ENGG2020 or ENGG2120 or ESTR2104.
                     For 2nd-year entrants, the prerequisite will be waived.

                     New Enrollment Requirement(s):
                     Pre-requisite = no change
                     Exclusion = no change

CAF

eLearning hrs for blended cls   0
No. of micro-modules   0
Research components (UG)   50%-74%

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