THE CHINESE UNIVERSITY OF HONG KONG Print Course Catalog Details

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Academic Org: Dept of Computer Sci & Engg - Subject: Computer Engineering

Course: CENG3410	Course ID: 011974	Eff Date: 2022-07-01	Crse Status: Active	Apprv. Status: Approved	[Course Rev]
Smart Hardware Design 智能硬	件設計				

This is a hands-on project-based course that introduces the devices, system architecture, communication protocol and design methodology needed for the design and construction of smart hardware systems. With the advent of affordable sensors and Internet of Things (IoT), smart hardware systems such as all sorts of wearable devices and smart home appliances are expected to significantly improve people's living style and enhance work efficiency. Students in this course will work in groups to develop small smart hardware systems, prototype their designs and testing them.

本科介紹智慧硬體中使用的器件、系統架構、通信協議以及設計方法。隨著感測器的普及以及物聯網的應用,智慧硬體(如各種可穿戴設備和智慧家居產品)將大大提高人們的生活品質和工作效率。本科的學生將以小組爲單元設計小型的智慧硬體,進行原型驗證和測試。

Grade Descriptor:

EXCELLENT – exceptionally good performance and far exceeding expectation in all or most of the course learning outcomes; demonstration of superior understanding of the subject matter, the ability to analyze problems and apply extensive knowledge, and skillful use of concepts and materials to derive proper solutions.

有關等級說明的資料,請參閱英文版本。

В

А

GOOD – good performance in all course learning outcomes and exceeding expectation in some of them; demonstration of good understanding of the subject matter and the ability to use proper concepts and materials to solve most of the problems encountered.

有關等級說明的資料,請參閱英文版本。

С

FAIR - adequate performance and meeting expectation in all course learning outcomes; demonstration of adequate understanding of the subject matter and the ability to solve simple problems.

有關等級說明的資料,請參閱英文版本。

D

MARGINAL - performance barely meets the expectation in the essential course learning outcomes; demonstration of partial understanding of the subject matter and the ability to solve simple problems.

有關等級說明的資料,請參閱英文版本。

F

FAILURE - performance does not meet the expectation in the essential course learning outcomes; demonstration of serious deficiencies and the need to retake the course.

有關等級說明的資料,請參閱英文版本。

Equivalent Offering:	
Units:	3 (Min) / 3 (Max) / 3 (Acad Progress)
Grading Basis:	Graded
Repeat for Credit:	Ν
Multiple Enroll:	Ν
Course Attributes:	

Topics:

	COURSE OUTCOMES			
Learning Outcomes:				
	At the end of the course of studies, students will have acquired the ability to1. Understand the limitations and benefits of various sensors used in smart hardware systems;2. Choose the right devices, system architecture, and communication protocol to implement a particular smart hardware system;3. Mange a small smart hardware development project.			
Course Syllabus:				
	Week 1: Introduction to smart hardware			
	Week 2-3: Microcontroller architecture and programming			
	Week 4-5: Sensors and applications			
	Week 6: Camera			
	Week 7: Actuator			
	Week 8-9: Communication (Bluetooth, Wifi, 3G, etc.)			

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	Week 10: Battery and low power design Week 11: Put it all together: smart band design Week 12-13: Student presentation					
Assessment Type:	Lab reports Others Presentation	: 20% : 60% : 20%				
Feedback for Evaluation:	 Quiz; Course evaluation and questionnaire; Question-and-answer sessions during class; Student consultation during office hours or Peer review; 	online;				
Required Readings:	-					
Recommended Readings:	Recommended Readings: 1. Ubiquitous Computing: Smart Devices, Environments and Interactions; 2. Make: Sensors: A Hands-On Primer for Monitoring the Real World with Arduino and Raspberry Pi;					
		OFFERINGS				
1. CENG3410	Acad Organization=CSD; Acad Career=	UG				
	LAB : Size=30; Final Exam=N; Contact= LEC : Size=30; Final Exam=N; Contact= TUT : Size=30; Final Exam=N; Contact=	COMPONENTS =1 =2 =1				
1. CENG3410	ENRO Enrollment Requirement Group: Not for students who have taken I New Enrollment Requirement(s): Exclusion = no change	LMENT REQUIREMENTS ERG3830.				

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CAF

eLearning hrs for blended cls 0 No. of micro-modules 0 Research components (UG) 0%

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