THE CHINESE UNIVERSITY OF HONG KONG
Print Course Catalog Details

Academic Org: Dept of Computer Sci & Engg – Subject: Computer Engineering

Course: CENG2010 **Course ID:** 010475 **Eff Date:** 2022-07-01 **Crse Status: Active** **Apprv. Status:** Approved **[**Course Rev**]**

Digital Logic Design Laboratory **數字邏輯設計實驗**

This course aims at providing an intensive hands-on introduction to digital system design using a hardware description language (e.g. VHDL). Students will learn how to design, simulate and debug digital systems through lab exercises. Topics include the basic language syntax, signals/variables/constants declaration, data types, basic operators, concurrent and sequential statements, and structural modelings.

本科旨在密集介紹如何利用硬件描述語言（如 VHDL）設計數位邏輯系統。學生透過實驗學習數字系統的設計、模擬及調試技巧。主題包括基本設計語言語法、信號／變數／常數申明、數據類型、基本運算符、共時性／順序性敘述，及結構建模。

Grade Descriptor:

A

EXCELLENT – exceptionally good performance and far exceeding expectation in all or most of the course learning outcomes; demonstration of superior understanding of the subject matter, the ability to analyze problems and apply extensive knowledge, and skillful use of concepts and materials to derive proper solutions.

有關等級說明的資料，請參閱英文版本。

B

GOOD – good performance in all course learning outcomes and exceeding expectation in some of them; demonstration of good understanding of the subject matter and the ability to use proper concepts and materials to solve most of the problems encountered.

有關等級說明的資料，請參閱英文版本。

C

FAIR – adequate performance and meeting expectation in all course learning outcomes; demonstration of adequate understanding of the subject matter and the ability to solve simple problems.

有關等級說明的資料，請參閱英文版本。

D

MARGINAL – performance barely meets the expectation in the essential course learning outcomes; demonstration of partial understanding of the subject matter and the ability to solve simple problems.

有關等級說明的資料，請參閱英文版本。

F

FAILURE – performance does not meet the expectation in the essential course learning outcomes; demonstration of serious deficiencies and the need to retake the course.

有關等級說明的資料，請參閱英文版本。

Equivalent Offering:
Units: 1 (Min) / 1 (Max) / 1 (Acad Progress)
Grading Basis: Graded
Repeat for Credit: N
Multiple Enroll: N
Course Attributes:

Topics:

COURSE OUTCOMES

Learning Outcomes:

At the end of the course of studies, students will have acquired the ability to
1. apply concepts and methods of digital system design techniques;
2. design combinational and sequential digital systems using hardware description language (HDL);
3. analyze the results of logic and timing simulations and debug digital systems.

Course Syllabus:

This course aims at providing an intensive hands-on introduction to digital system design using a hardware description language (e.g. VHDL). Students will learn how to design, simulate and debug digital systems through lab exercises. Topics include the basic language syntax, signals/variables/constants declaration, data types, basic operators, concurrent and sequential statements, and structural modelings.

Assessment Type:

Essay test or exam	: 50%
Others	: 50%

Feedback for Evaluation:

1. Course evaluation and questionnaire;
2. Results of assignments and examination;
3. Question-and-Answer sessions during class;
4. Student consultation during office hours or online;

Required Readings:

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Recommended Readings:

1. Digital Design with RTL Design, VHDL, and Verilog, 2/e, by Frank Vahid;
2. VHDL for Digital Design, by Frank Vahid & Roman Lysecky

OFFERINGS

1. CENG2010 Acad Organization=CSD; Acad Career=UG

COMPONENTS

LAB : Size=30; Final Exam=N; Contact=1
LEC : Size=30; Final Exam=Y; Contact=1

ENROLMENT REQUIREMENTS

CAF

eLearning hrs for blended cls 0
No. of micro-modules 0
Research components (UG) 0%

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