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CEG5010 Reconfigurable Computing

FPGA Interconnect

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Introduction

- Interconnect most important as it accounts for most of the area and delay in an FPGA
- Discuss 2 examples
 - Very simple island-style FPGA interconnect (Vaughn Betz)
 - Single directional drivers which are an improvement (Guy Lemieux)

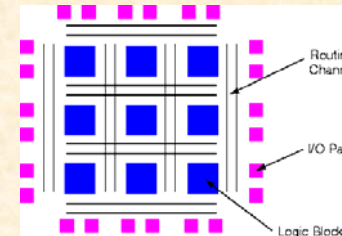
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Simple FPGA Interconnect

Thanks to Vaughn Betz for permission to use his figures from http://www.eecg.toronto.edu/~vaughn/challenge/fpga_arch.html in this lecture.

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Review: Island Style FPGA

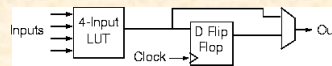


Uniform channels, 2 pads per row or column.
 io_rat 2
 chan_width_io 1
 chan_width_x uniform 1
 chan_width_y uniform 1

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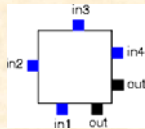
Basic Logic Element

- Assume no clusters (N=1)



subblocks_per_clb 1
subblock_lut_size 4

- Inputs come in on a side but the output can connect to the right or below

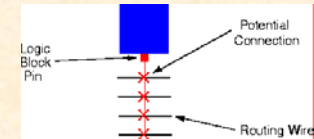


inpin class: 0 bottom
inpin class: 0 left
inpin class: 0 top
inpin class: 0
right outpin class: 1 bottom right

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Connection Block

- W=channel width
- Fc=number of channel wires to which each logical pin can connect
- In the slide, what is W and Fc?

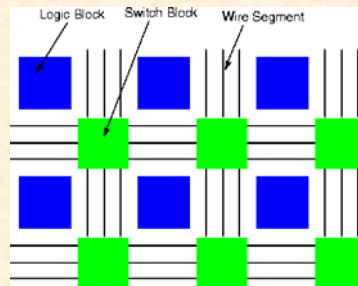


Fc_type fractional
Fc_output 1
Fc_input 1
Fc_pad 1

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Routing

- This is unsegmented, each wiring segment spans only 1 logic block
- Switch box switches are used to connect segments and make longer wires

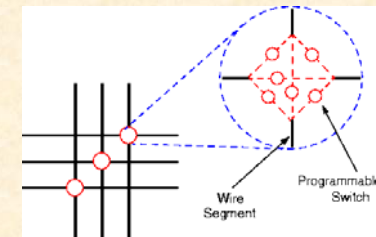


segment frequency: 1 length: 1 wire_switch: 0 opin_switch: 0 Frac_cb: 1. \ Frac_sb: 1. Rmetal: 4.16 Cmetal: 81e-15

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Switch Box

- Fs=total number of connections offered to each incoming wire (what is Fs in the figure?)
- The topology shown here is called "planar" or "domain-based," others are possible
- Question: can you have different topologies for the same Fs? Would that affect routability?

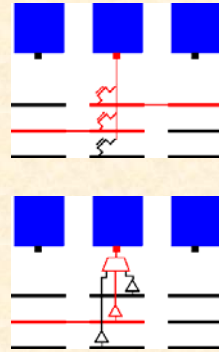


switch_block_type subset

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Input pin doglegs

- Input pin doglegs to logic blocks are not allowed as implementation is not pass transistor based
- Actual implementation has buffers and muxes
- Hence cannot use this to change tracks



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Thanks to Guy Lemieux for permission to use his slides in this lecture.

Directional and Single-Driver Wires in FPGA Interconnect

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G. Lemieux, E. Lee, M. Tom, and A. Yu, "Directional and Single-Driver Wires in FPGA Interconnect", *IEEE International Conference on Field-Programmable Technology*, Brisbane, Australia, pp. 41-48, December 2004.

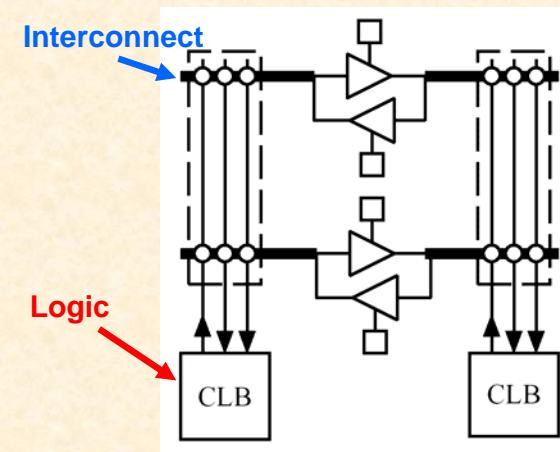
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Outline

- Motivation
- Bidirection vs. Directional
 - New detailed routing architecture
 - Which is better?
- Tristate vs. Single-Driver
 - HSPICE results
 - Which is better?
- Place & Route Results
- Conclusions

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Motivation: Bidirectional Wires



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Motivation: Bidirectional Wires

Problem

Half of **Tristate Buffers** Left Unused

Buffers **Dominate** Size of Device

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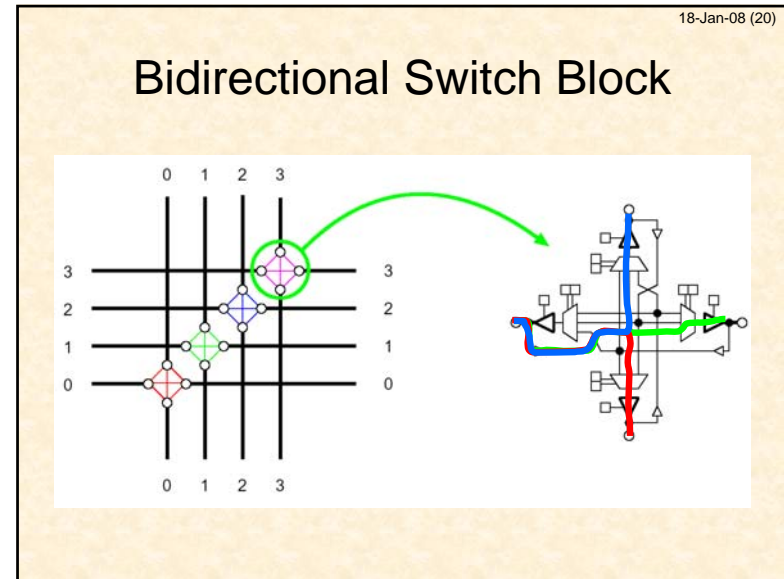
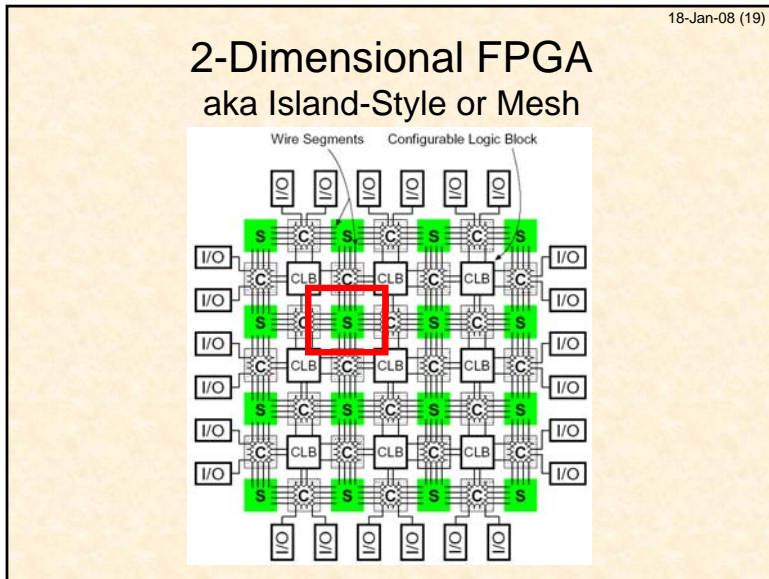
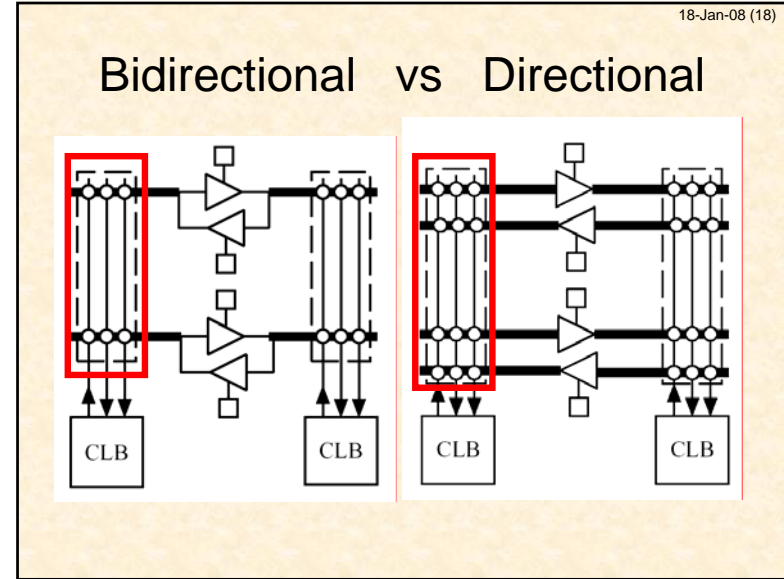
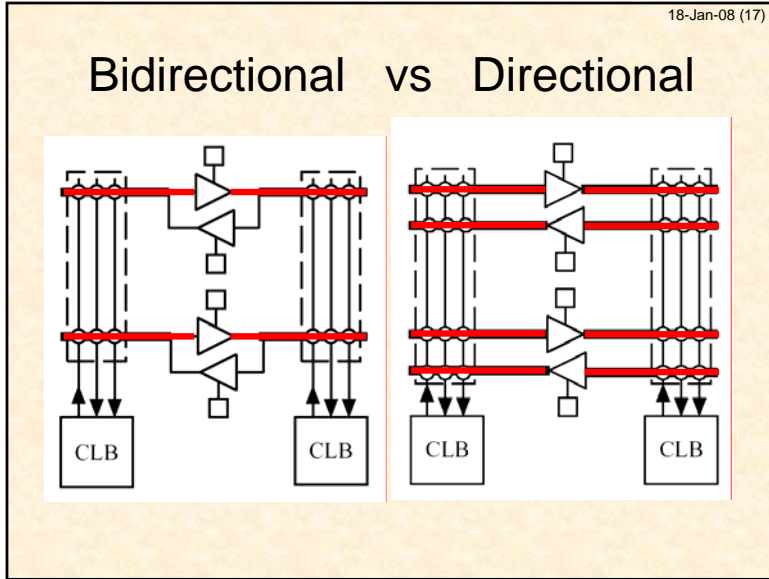
Bidirectional vs. Directional Wiring

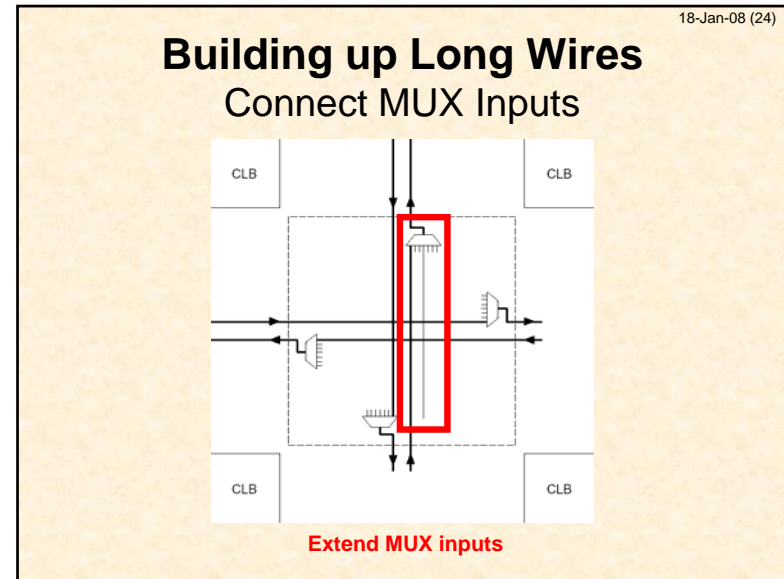
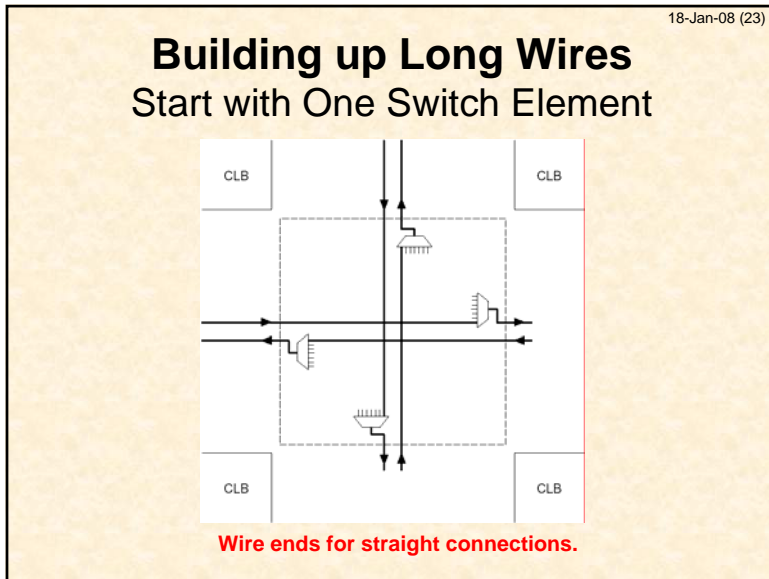
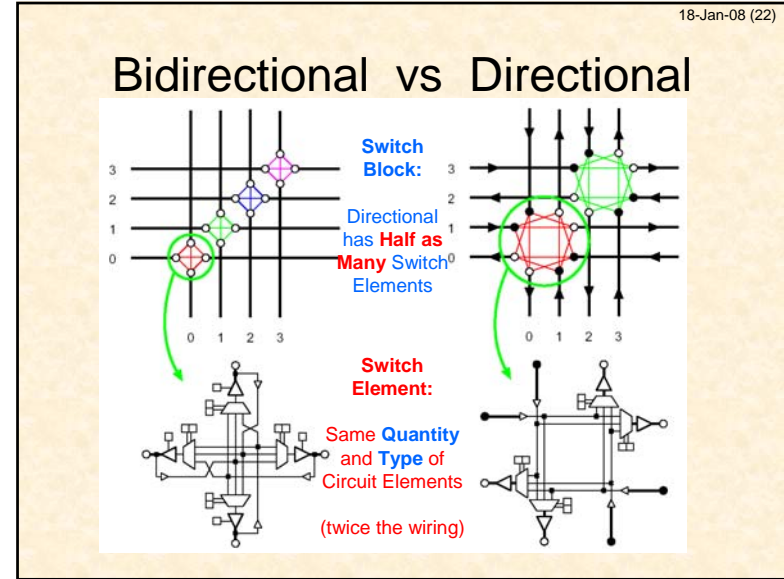
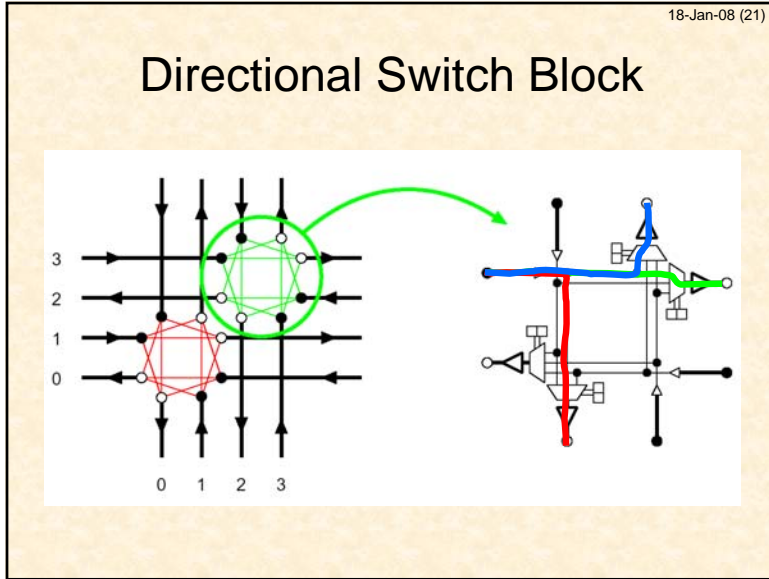
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Bidirectional vs Directional

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Bidirectional vs Directional





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Building up Long Wires

Connect MUX Inputs

TURN UP from wire-ends to mux

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Building up Long Wires

Connect MUX Inputs

TURN DOWN from wire-ends to mux

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Building up Long Wires

Add +2 More Wires (4 total)

Add LONG WIRES, turning UP and DOWN.

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Building up Long Wires

Add +2 More Wires (6 total)

Add LONG WIRES, turning UP and DOWN.

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Building up Long Wires Single Layout Tile !!!

Add wire twisting

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Long Wires!

1 2 3

NOTICE: One switch element holds 6 wires
 $\#Wires := WireLength \times NumDirections = 3 \times 2 = 6$

No "partial" switch elements with fewer wires

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Small Switch Block One L3 Switch Element

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Bigger Switch Block Two L3 Switch Elements

NOTICE
 Switch element design forces **quantization** of channel width

Bidirectional
 One quantum = $1 * L$

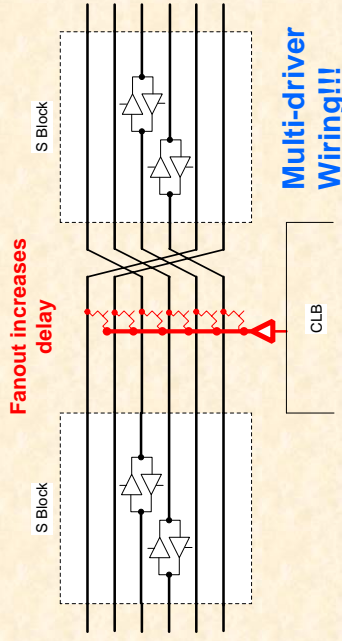
Directional
 One quantum = $2 * L$

Summary

- Directional wiring
 - Good
 - Potential area savings
 - Bad
 - Big input muxes, slower
 - Bigger quantum size (2*L)
 - Detailed-routing architecture is different (need new switch block)
- Need to evaluate!

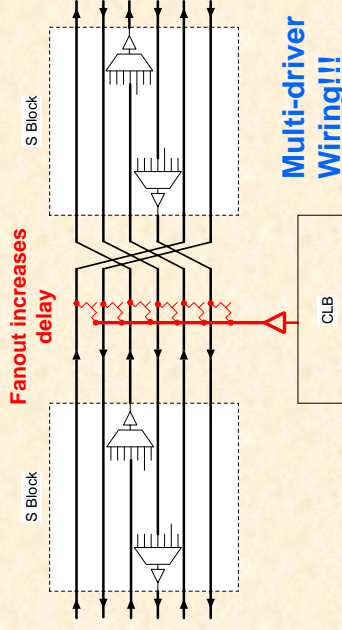
Tristate vs. Single-driver Wiring

Bidirectional Wiring Outputs are Tristates

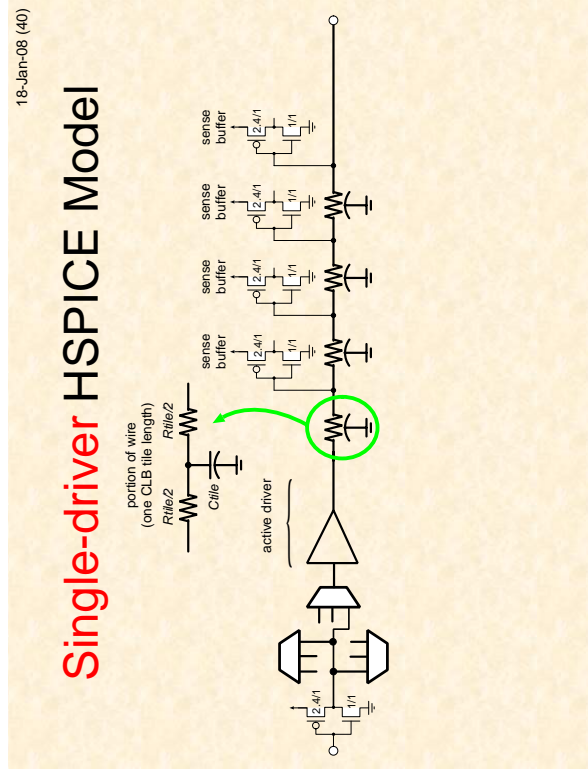
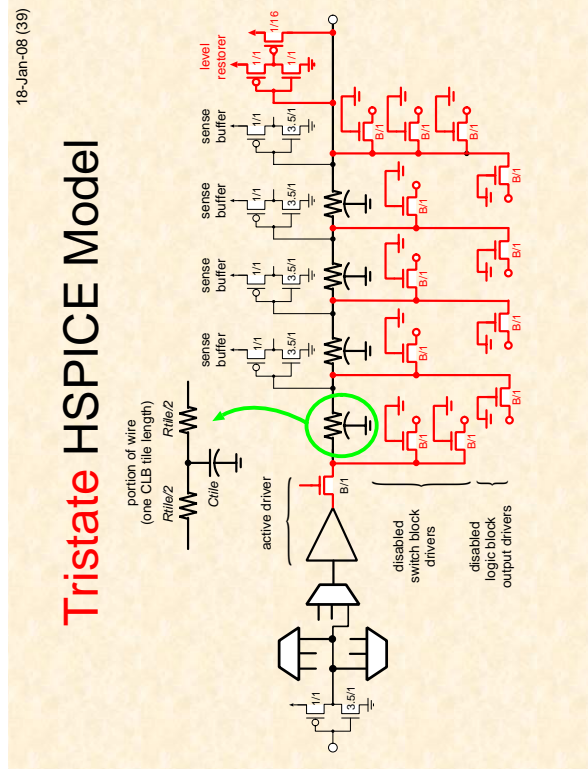
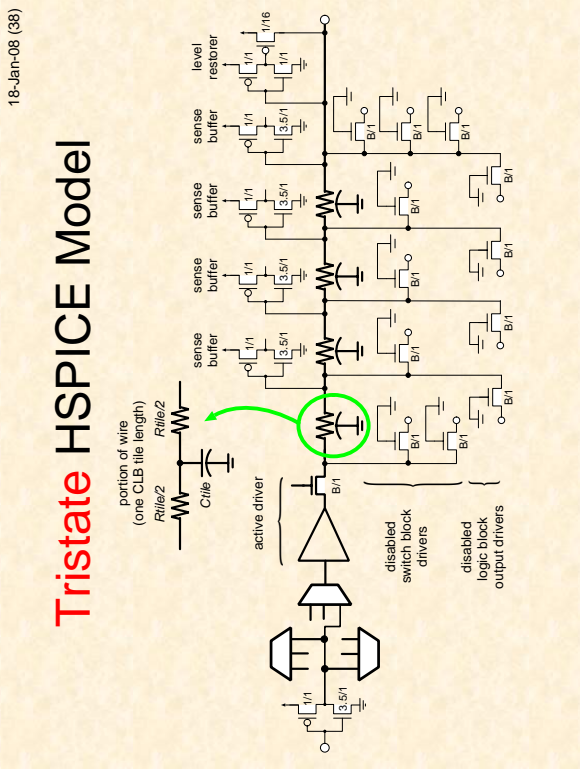
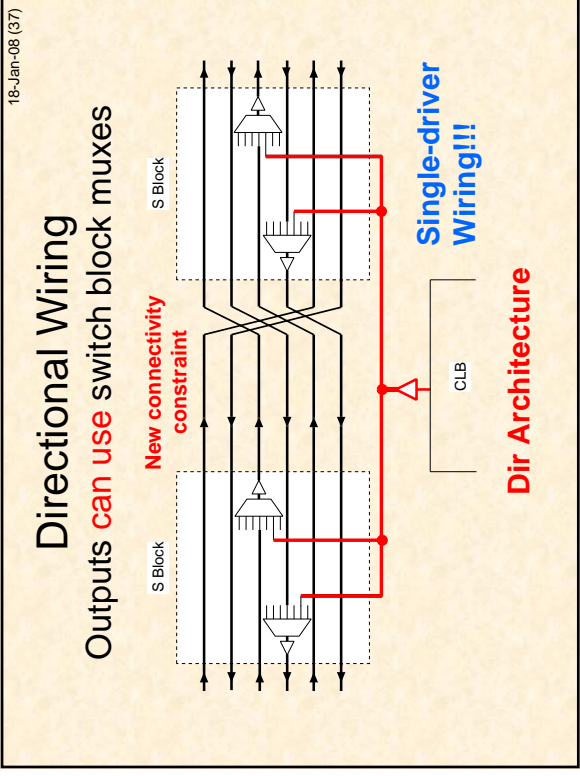


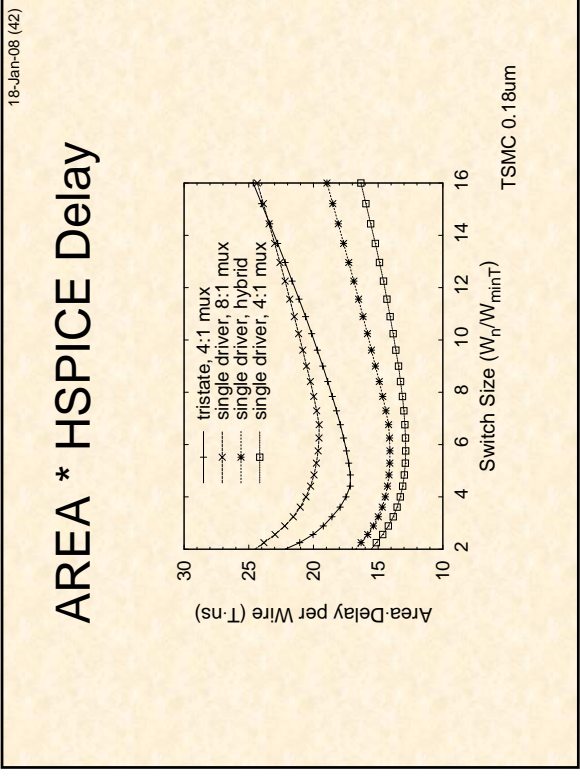
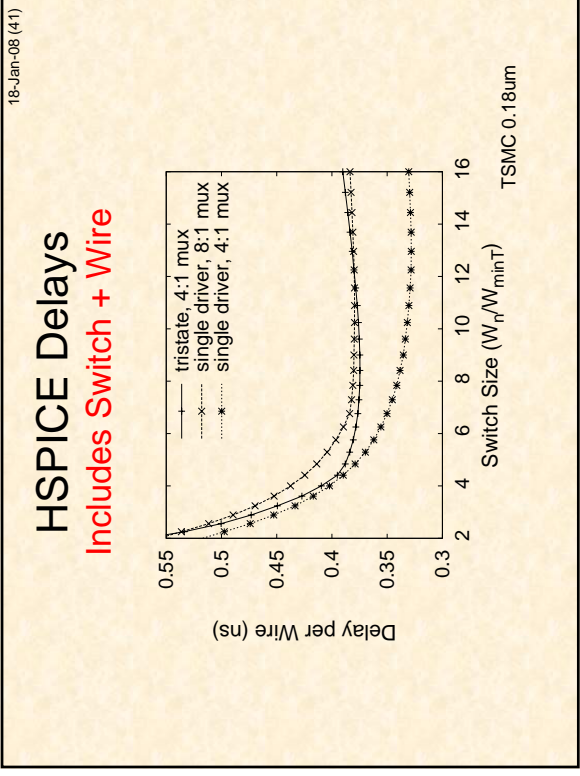
Bidir Architecture

Directional Wiring Outputs can be Tristates



Dir-Tri Architecture





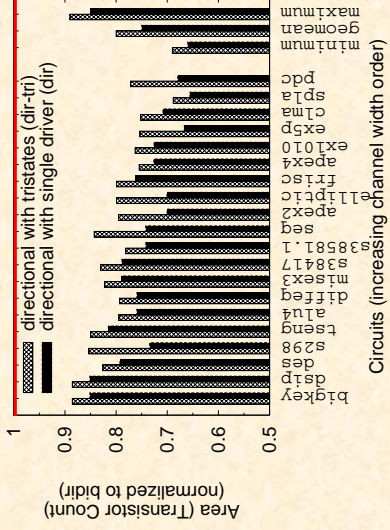
- 18-Jan-08 (43)
- ### Summary
- Single-driver wiring
 - Good
 - Same delay as tristate
 - No delay increases caused by fanout
 - Fewer wire loads: 27% lower capacitance
 - Bad
 - Directional only (by necessity)
 - Area-delay product "seems" worse, but isn't

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Place and Route Results

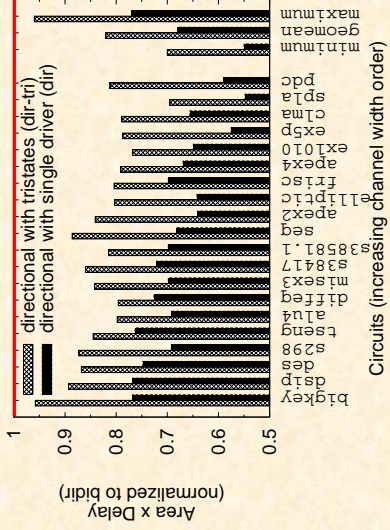
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Area (Transistor Count)



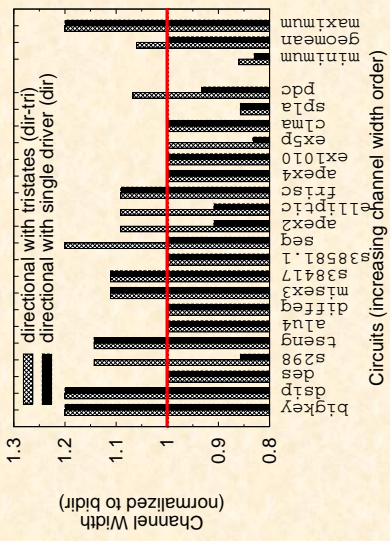
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Area-Delay Product



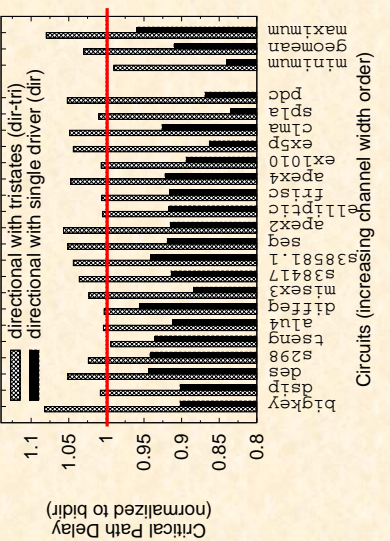
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Channel Width



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Delay



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Results Summary

- Average improvements using **single-driver wiring**
 - 0% channel width
 - 9% delay
 - 14% tile length of physical layout
 - 25% transistor count
 - 32% area-delay product
 - 37% wiring capacitance

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Conclusions

- No more tristates!
 - Eliminates need for pass transistors
 - No “Vt” loss signal degradation
 - Better signal reliability, better drive strength
- Significant savings in all metrics
 - Any reasons left to use bidirectional wiring ???
- Savings **INCREASES** with circuit size
 - Because interconnect dominates big circuits

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Review Questions

- What are the advantages and disadvantages of single vs bidirectional drivers?
- Why did they need to test the design with different benchmarks? Couldn't they just measure the speed and area of the two different designs?
- For the tristate buffer, why is the P:N ratio of the sense buffer 1:3.5?

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References

- Architecture and CAD for Deep-Submicron FPGAs, V. Betz, J. Rose, and A. Marquardt, Kluwer Academic Publishers, February 1999. 264 pages.
- http://www.eecg.toronto.edu/~vaughn/challenge/fpga_arch.html
- G. Lemieux, E. Lee, M. Tom, and A. Yu, “Directional and Single-Driver Wires in FPGA Interconnect”, *IEEE International Conference on Field-Programmable Technology*, Brisbane, Australia, pp. 41-48, December 2004.