

FPGA Architectures

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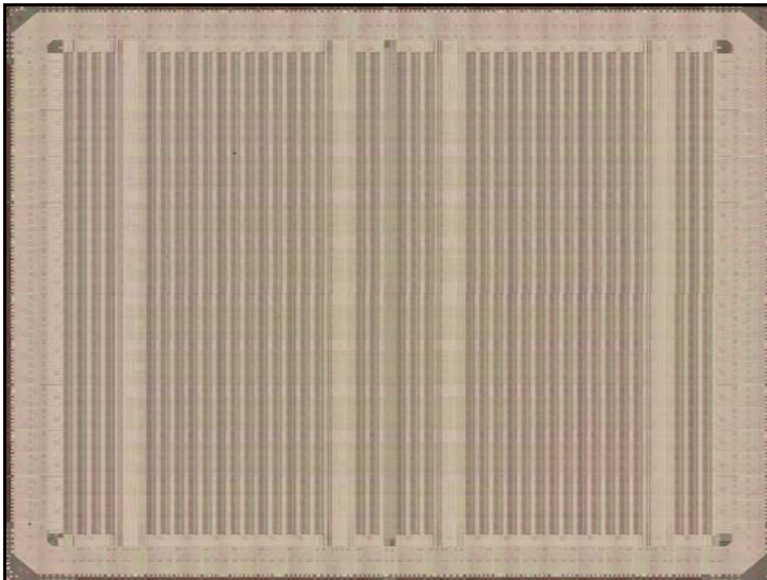
Course web site: <http://www.ece.ubc.ca/~eece583>

But this isn't an architecture course?!?!?

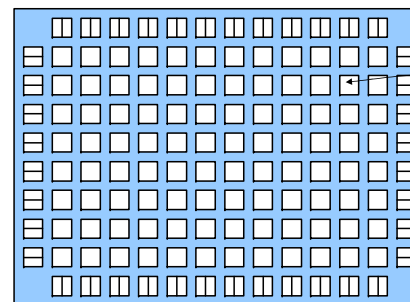
A lot of the CAD algorithms we will talk about are specific to FPGAs:

- FPGAs consume a large market share of all CAD
- Their structure provides unique CAD constraints and opportunities
- As technology advances, we are seeing more "structured" approaches, even for custom-chip implementations
 - These will require new CAD techniques that may be inspired by those used for FPGAs today

Since we will spend a lot of time talking about CAD for FPGAs, it is important to talk about what an FPGA looks like inside ("architecture")



What's Inside an FPGA?

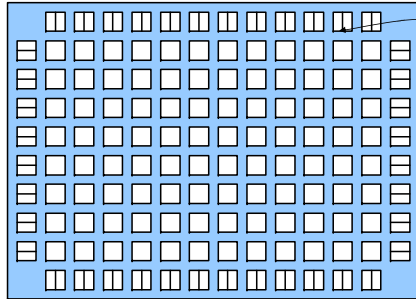


Logic Blocks
- used to implement logic
- lookup tables and flip-flops

Altera: LABs

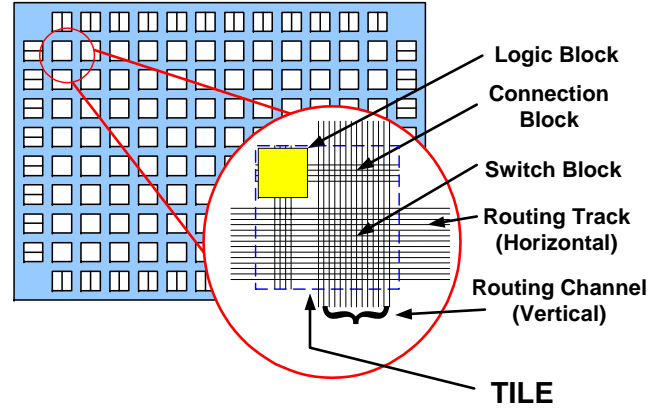
Xilinx: CLBs

What's Inside an FPGA?



I/O Blocks
- interface off-chip
- can usually support many I/O Standards

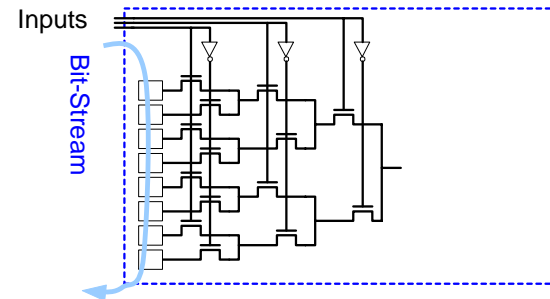
What's Inside an FPGA?



Logic Blocks implement the functionality of the circuit

Logic Block:

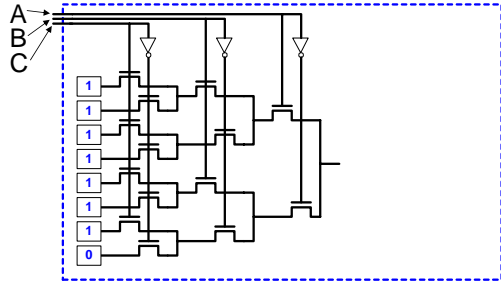
Basic Logic Gate: Lookup-Table



Function of each lookup table can be configured by shifting in bit-stream.

Logic Block:

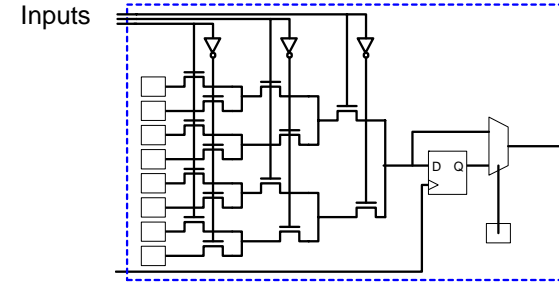
Quick Question: What function would this implement?



$$F = A + B + C$$

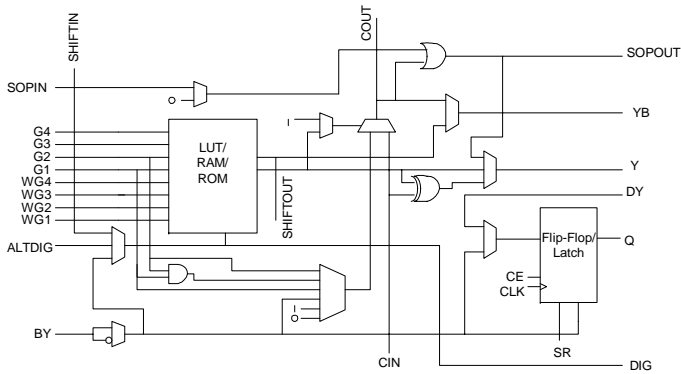
Logic Block:

Basic Logic Gate: Lookup-Table



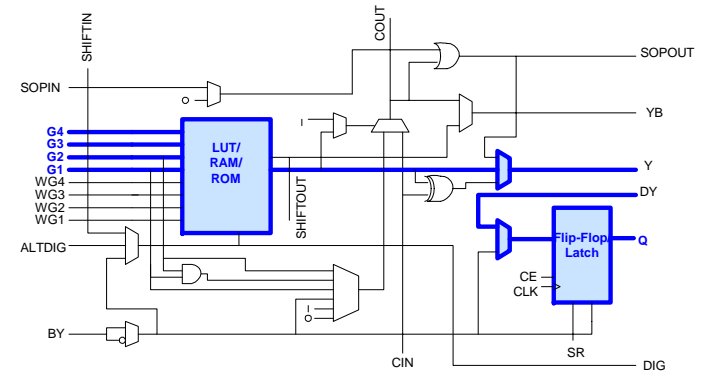
Function of each lookup table can be configured by shifting in bit-stream.

Xilinx Virtex II Logic Block



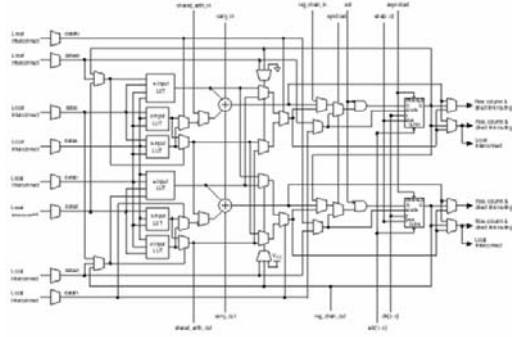
X 2

Xilinx Virtex II Logic Block



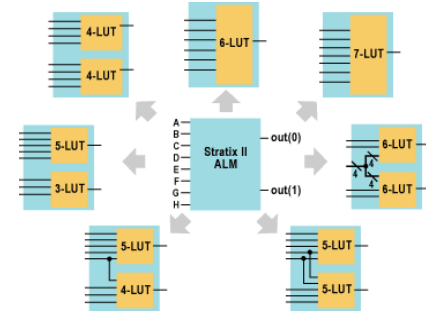
X 2

Stratix II Logic Block:



Source: Stratix II Handbook, 2005

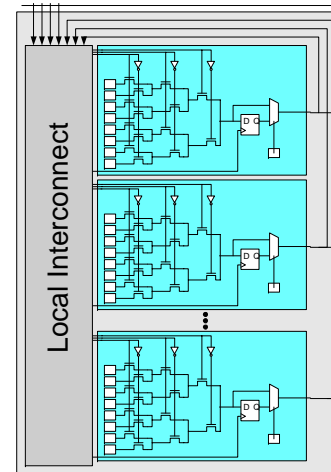
Stratix II Logic Block:



Source: Stratix II Handbook, 2005

Logic Blocks are grouped into Clusters

Logic Clusters



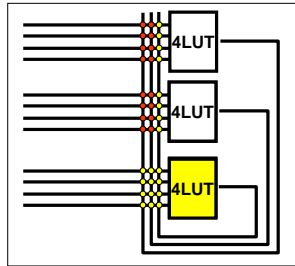
Intra-cluster connections: fast

Inter-cluster connections: slow

There is a balance:

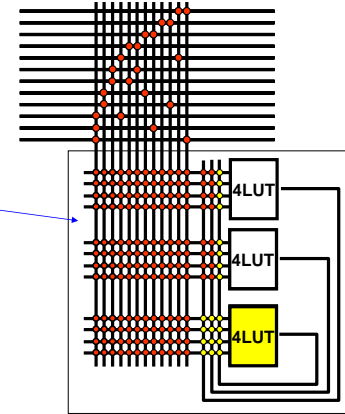
- Larger clusters mean more intra-cluster connections
- But, larger clusters means the intra-cluster connections are not as fast

Cluster Architecture:



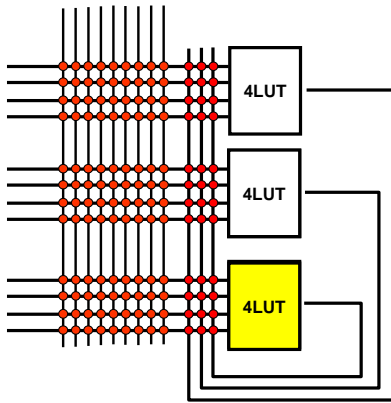
Cluster Architecture:

This will significantly impact the speed and routability of the device



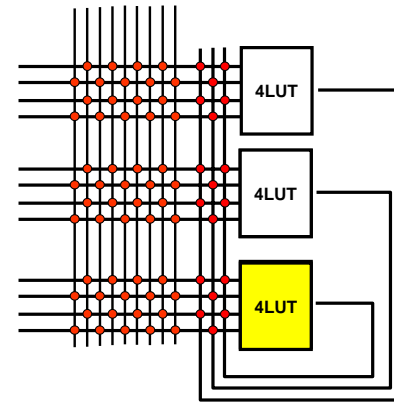
Intra-cluster routing:

Academic studies typically consider fully populated:

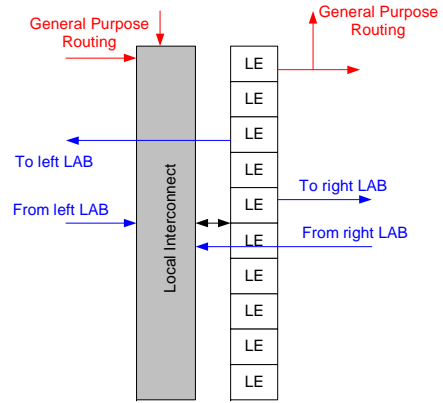


Intra-cluster routing:

Commercial parts: depopulated (this is 50%)



Altera Stratix LAB (Logic Array Block):

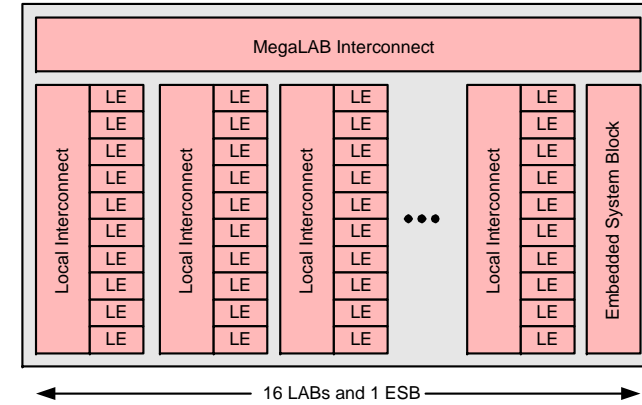


10 Logic Elements in each LAB

Two carry chains through each LAB

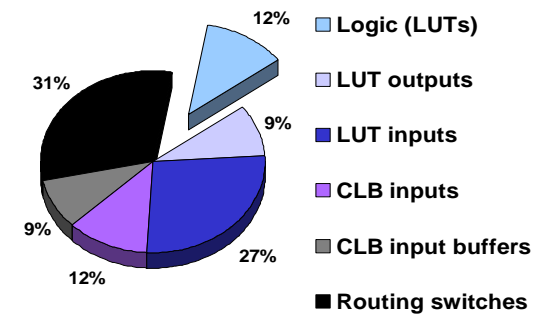
Connections to general purpose routing and neighbouring LABs

Altera APEX MegaLAB:



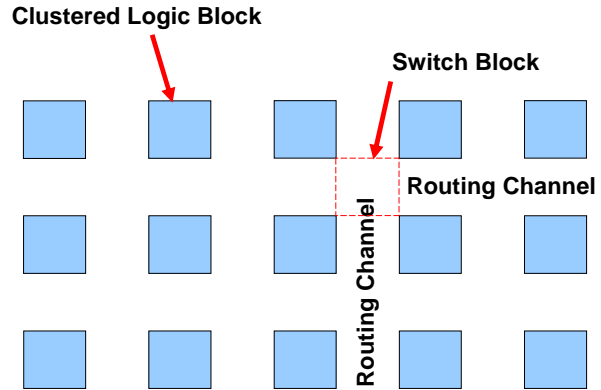
Routing Fabric

Routing is important!

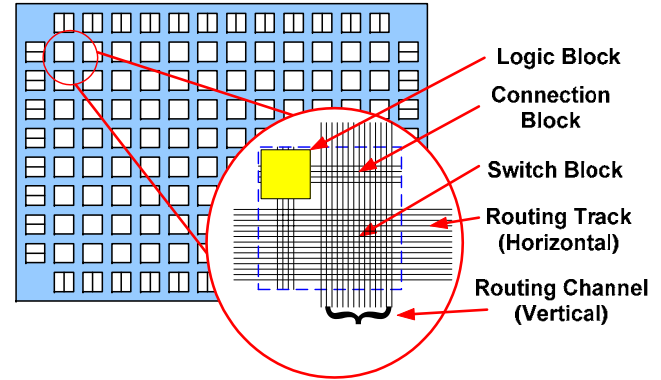


Source: Guy Lemieux

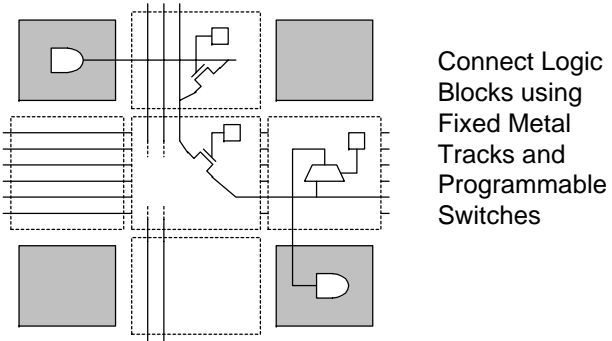
Mesh (Island-style) FPGA



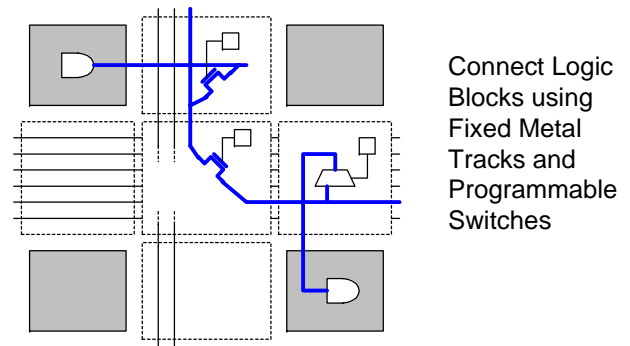
What's Inside an FPGA?



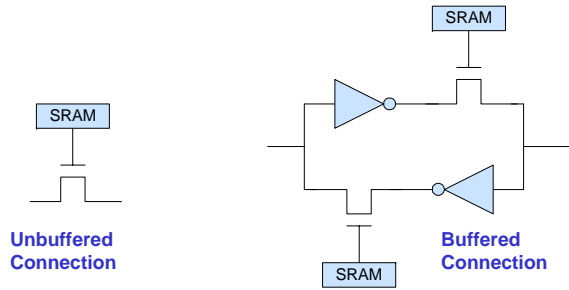
Reconfigurable Logic:



Reconfigurable Logic:

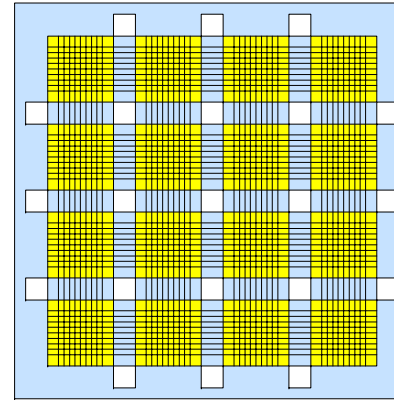


Programmable Switches



Today, buffered connections are common

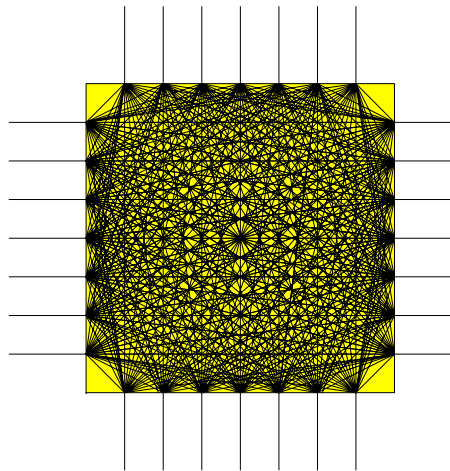
Switch Blocks



Most of the FPGA area is due to routing

- Fixed metal tracks arranged in horizontal and vertical channels
- Connected to each other using switch blocks

Switch Blocks:

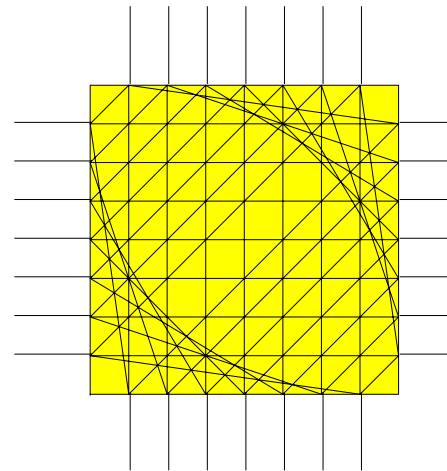


Switch Blocks connect horizontal and vertical channels

Every possible connection?

- Too big
- Too slow

Switch Blocks:



Switch Blocks connect horizontal and vertical channels

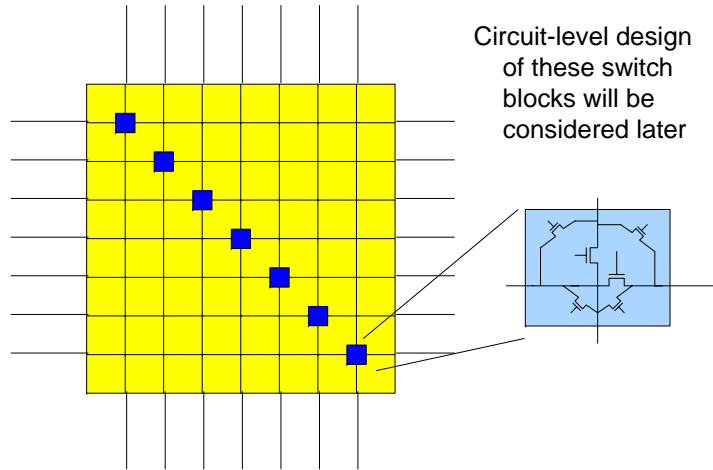
Every possible connection?

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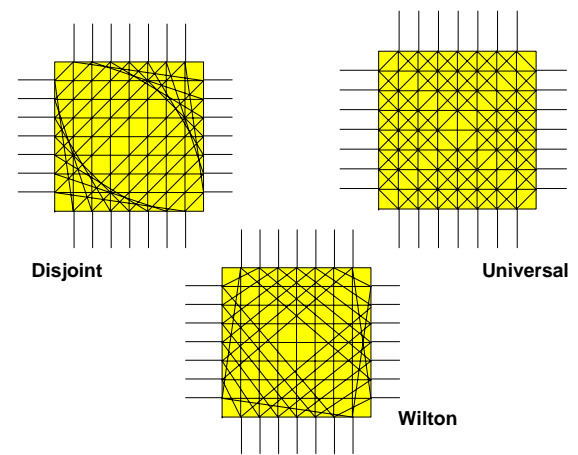
Many Topologies possible

$F_s = 3$ is common

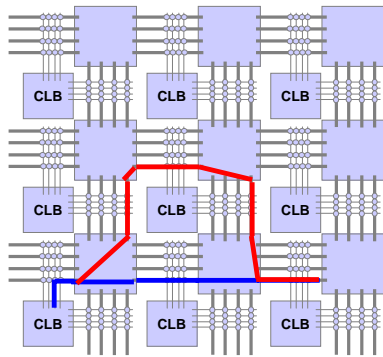
Implementing the Switch Block:



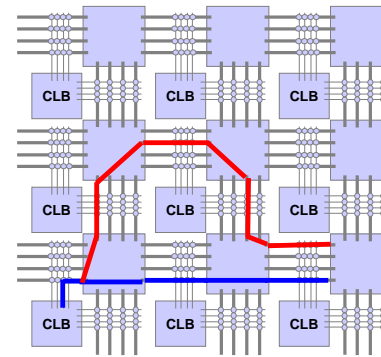
Switch Block Topologies:



Advantage of Wilton Switch Block



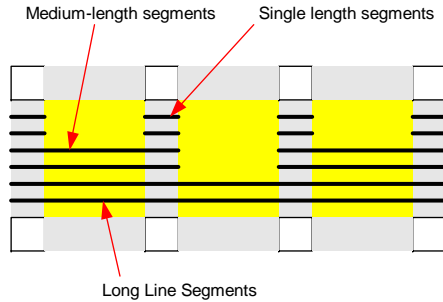
Advantage of Wilton Switch Block



Diversity means you can "get to" more routing tracks.

It tends to provide slightly better routability. No big impact on delay.

Wiring Segments



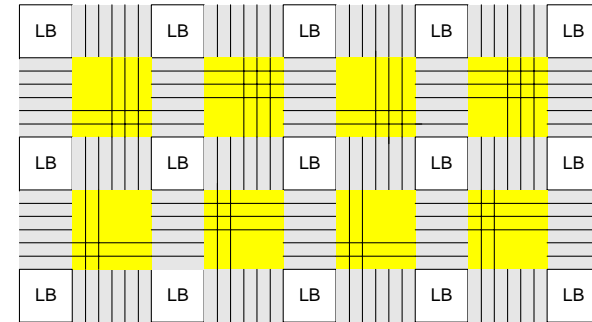
Short segments are good for local connections

Long segments are good for global connections

Most FPGA's have a variety of segment lengths

Segmented Architecture

At each switch block: some tracks end
some tracks pass right through



Segment Lengths

Typically, an FPGA contains a mix of segment lengths:

- Some wires that span only one logic block
- Some wires that span more than one logic block
- Some wires that span the whole chip

If a segment is too short, must traverse many segments to reach your destination

If a segment is too long, waste routing capacity, extra capacitance

Academic work has suggested [length-4](#) segments

Wilton block for Segmented Architectures

Wilton block needs more switches for pass through case

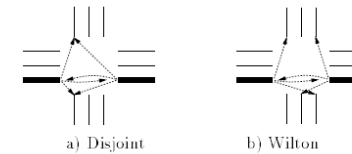


Fig. 3. Wire terminates at switch block

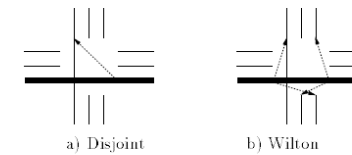
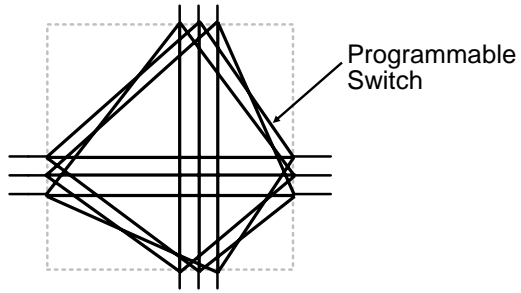


Fig. 4. Wire passes through switch block

The "Imran" Switch Block

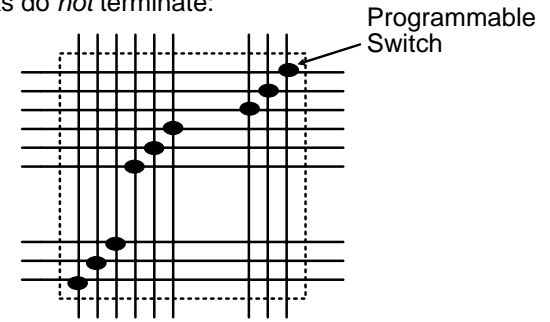
At each Switch Block, some tracks terminate:



Connect using "Wilton" pattern

The "Imran" Switch Block

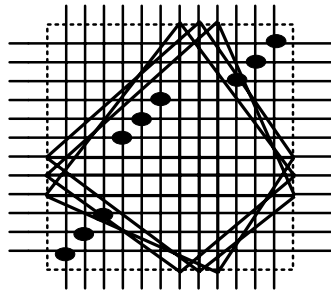
Some tracks do *not* terminate:



Connect using "Disjoint" pattern

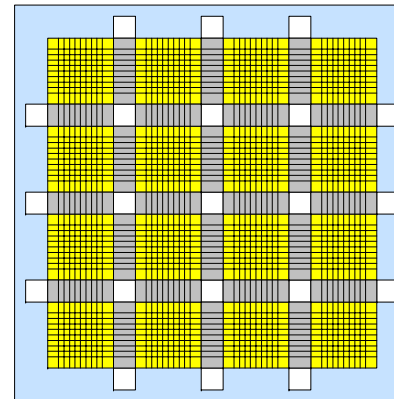
The "Imran" Switch Block

Put the two together:



Gives good results for segmented architectures

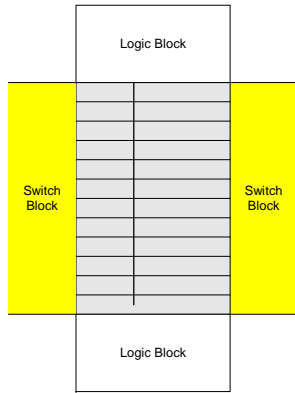
Connection Blocks



Most of the FPGA area is due to routing

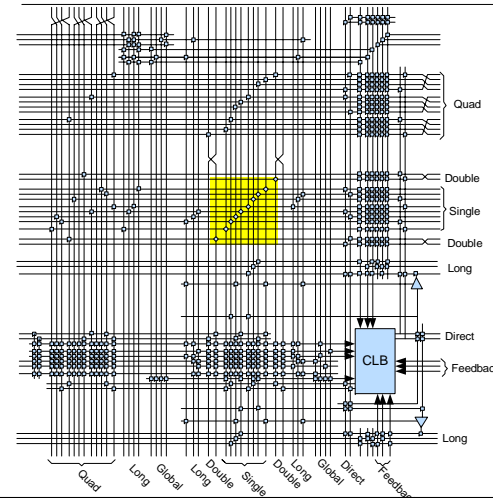
- Fixed metal tracks arranged in horizontal and vertical channels
- Connected to each other using switch blocks
- Connected to logic blocks using connection blocks

Connection Block



Each pin can connect to a subset of the tracks in an adjacent channel

Detailed Routing Diagram (XC4000X)



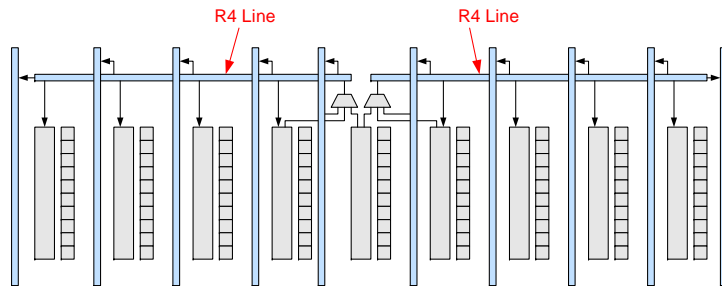
Dots represent Programmable Connections

Yes, this is old, but it illustrates the parts.

Today, vendors don't publish the routing details

Altera Stratix

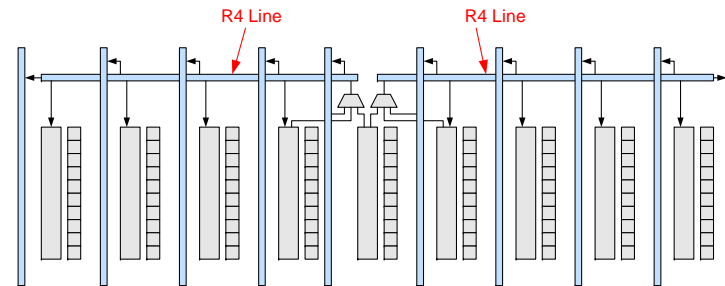
Horizontal: R4 Lines, R8 Lines, R28 Lines
 Vertical: C4 Lines, C8 Lines, C16 Lines
 Local Interconnects



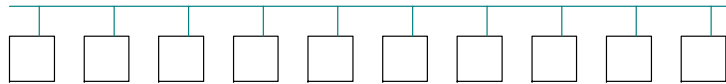
Altera Stratix II

Horizontal: R4 Lines, R24 Lines
 Vertical: C4 Lines, C16 Lines
 Local Interconnects

They found little benefit to the length-8 lines in Stratix



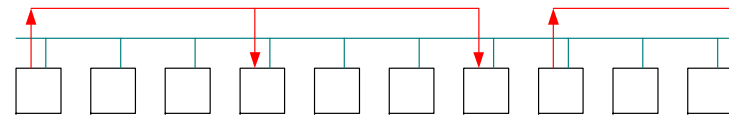
Xilinx Virtex II:



Long Lines: Span entire chip

- 24 in each channel (horizontal and vertical)
- Can connect to any logic block (actually through the neighbouring switch block)

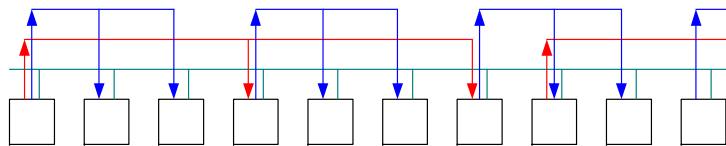
Xilinx Virtex II:



Hex Lines:

- 120 in each channel (horizontal and vertical)
- Can only be driven at one end
- Two connections to destination logic blocks

Xilinx Virtex II:

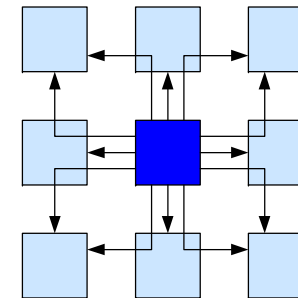


Double Lines

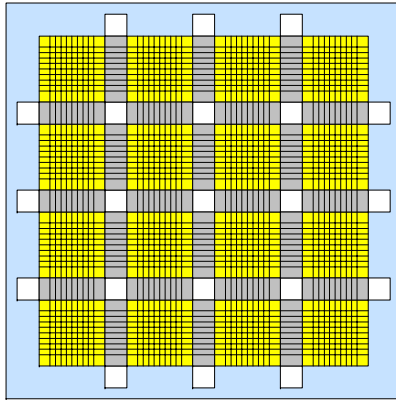
- 40 in each channel (horizontal and vertical)
- Driven at one end

Xilinx Virtex II:

Local Interconnect between neighbouring logic blocks:



Connection Blocks

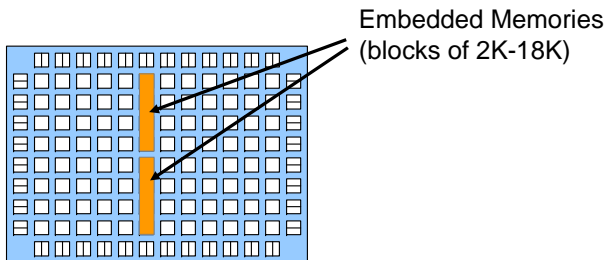


- Most of the FPGA area is due to routing
- Fixed metal tracks arranged in horizontal and vertical channels
 - Connected to each other using switch blocks
 - Connected to logic blocks using connection blocks

Systems

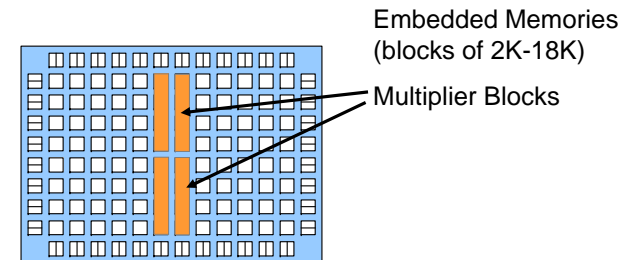
Implementing Systems in an FPGA:

FPGA vendors embed fixed blocks to improve speed and density:



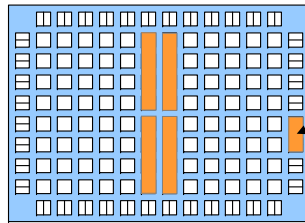
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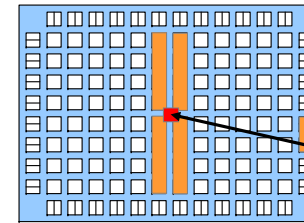
Embedded Memories
(blocks of 2K-18K)

Multiplier Blocks

High-Speed I/Os

Implementing Systems in an FPGA:

FPGA vendors embed fixed blocks to improve speed and density:



Embedded Memories
(blocks of 2K-18K)

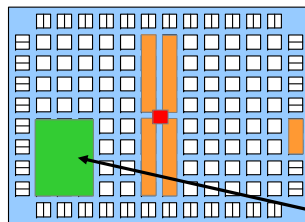
Multiplier Blocks

High-Speed I/Os

Dedicated Clock
Circuitry

Implementing Systems in an FPGA:

FPGA vendors embed fixed blocks to improve speed and density:



Embedded Memories
(blocks of 2K-18K)

Multiplier Blocks

High-Speed I/Os

Dedicated Clock
Circuitry

CPU (eg. ARM, MIPS)

Summary

Two Sources of Flexibility in an FPGA:

1. Most FPGAs use Lookup-Tables as their basic logic resource
 - 4-LUT can implement any function of 4 inputs
2. Connections between logic blocks can be made using fixed metal tracks
 - these fixed tracks are connected to each other and to the logic blocks using programmable switches