

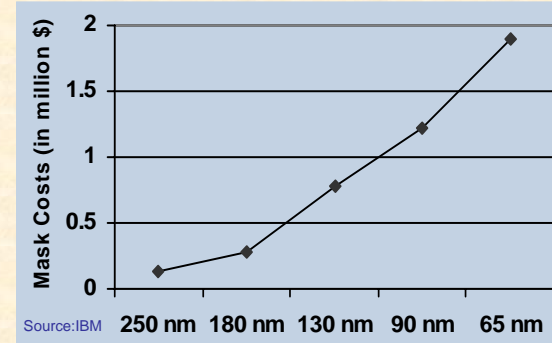
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## CEG 5010: Reconfigurable Computing ASICs vs FPGAs

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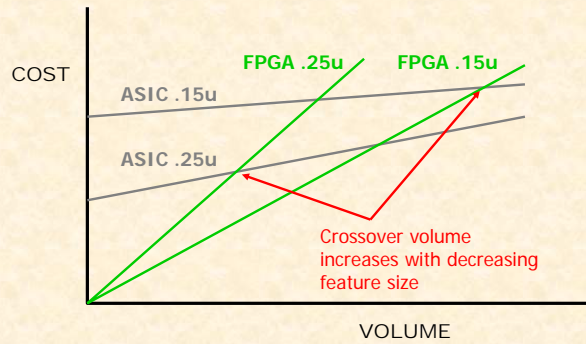
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## ASIC NRE



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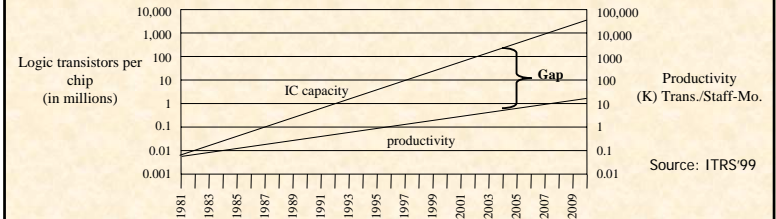
## Cost of Technology vs Volume

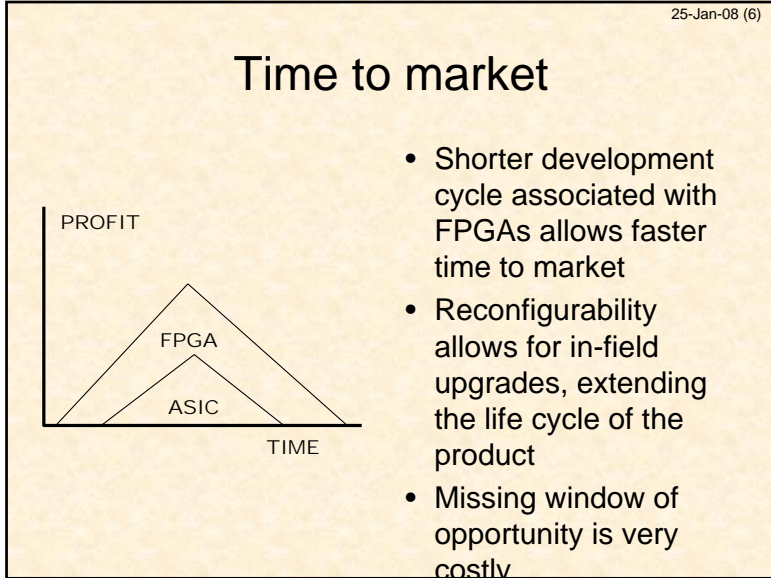
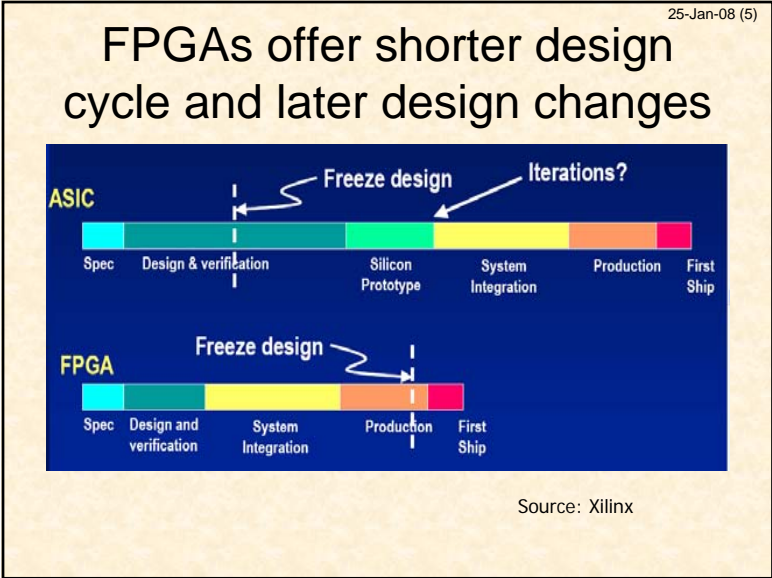


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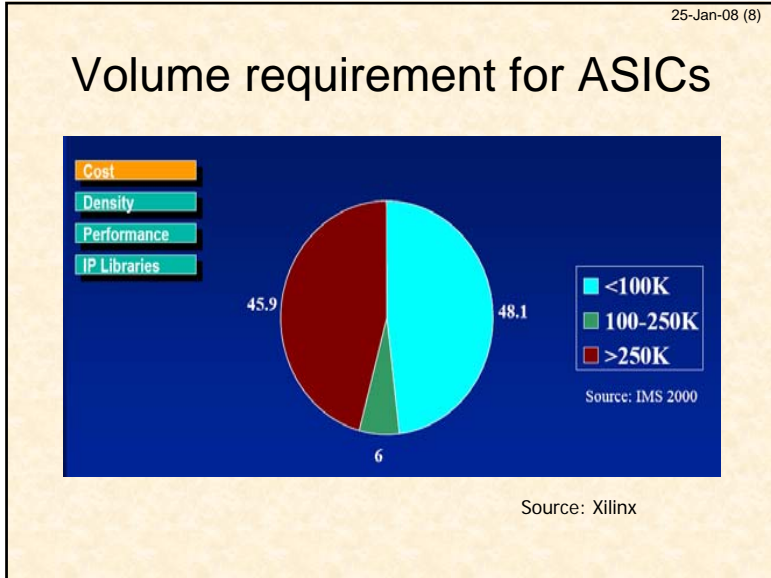
## Who can afford High-end ICs?

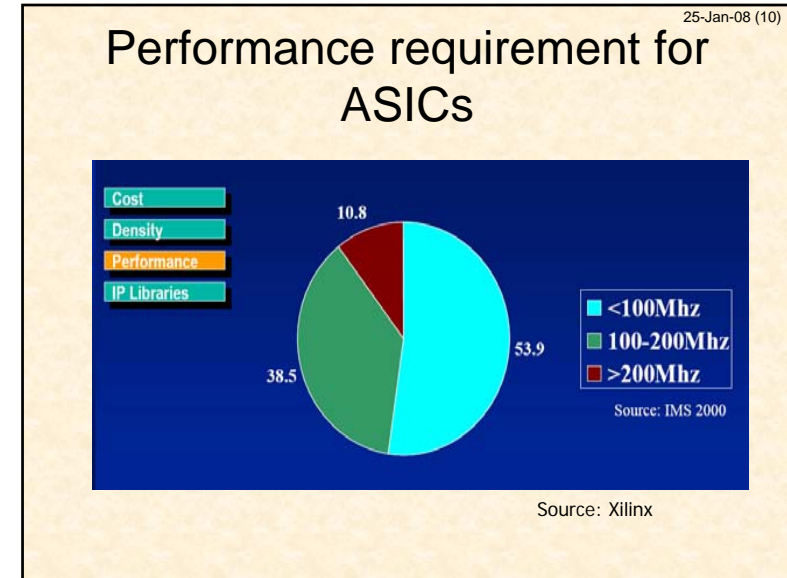
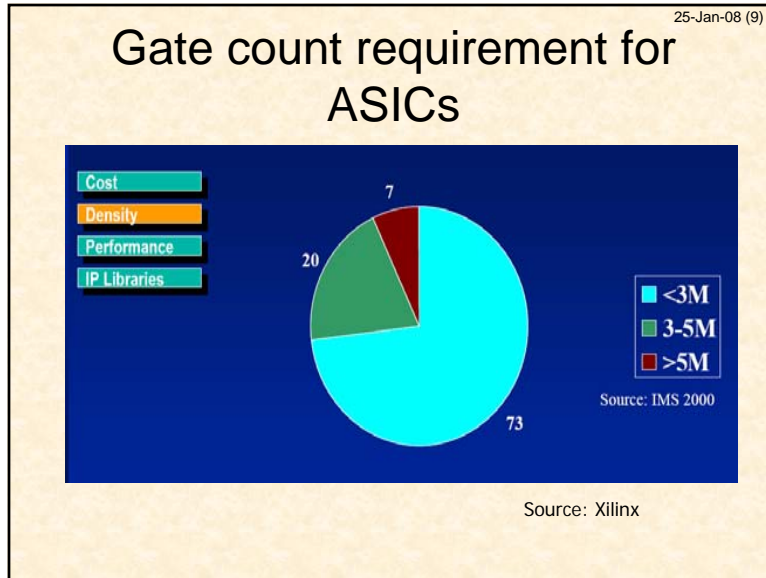
- ASICs becoming only for extreme designs, volume, speed, size, low power
- Design cost is another issue (1981: 100 designer months → ~\$1M 2002: 30,000 designer months → ~\$300M) Design productivity gap





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- ## Why do people use ASICs
- Cost
  - Density
  - Performance
  - IP Libraries





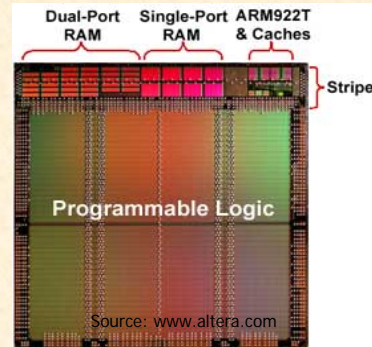
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- ## IP libraries
- Trend is to embed useful IP on the FPGA
    - uP, multipliers, transceivers, DLLs, RAM, IO standards, DDR, impedance control
  - IP/Core libraries
    - Implemented on the FPGA core e.g. FFT, PCI express, DDR ram controllers etc
  - Domain-specific languages e.g. System Generator translates between MATLAB/Simulink and FPGA circuits

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- ## IP Libraries: Xilinx Example
- Xilinx Virtex II Pro
  - PowerPC based
    - 420 Dhrystone MIPS at 300 MHz
    - 1 to 4 PowerPCs
    - 4 to 16 gigabit transceivers
    - 12 to 216 multipliers
    - 3,000 to 50,000 logic cells
    - 200k to 4M bits RAM
    - 204 to 852 I/O
    - \$100-\$500 (>25,000 units)
- 
- Up to 16 serial transceivers  
• 622 Mbps to 3.125 Gbps
- PowerPCs  
Config logic
- Courtesy of Xilinx

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## IP Libraries: Altera Example

- Altera's Excilibur EPXA 10
- ARM (922T) hard core
- ~200 Dhrystone MIPS at ~200 MHz
- Devices range from ~200k to ~2 million programmable logic gates



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## Example: DSP (2002)

Function	Industry's Fastest DSP Processor Core	
8 x 8 Multiply Accumulate	8.8 Billion MACs/s	0.5 Tera MACs/s
FIR Filter 256-tap Linear phase 16-bit data/coefficients	17 MSPS 1.1 GHz	180 MSPS 160 MSPS
FFT 1024 point 16-bit data	7.7 $\mu$ s 800 MHz	< 1 $\mu$ 140 MHz

Source: Xilinx

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## FPGA Area Efficiency

- FPGAs use more transistors
  - Does not mean higher yield any more because die are becoming pad limited (can't pack more die on a wafer)
  - We have more transistors than we can (afford to) design anyway
  - What about power?
- FPGAs about 40x area (20x with embedded blocks) and 3-4x slower than ASICs – is this important?

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## Conclusions

- The prohibitive costs of advanced IC technology means more and more low-medium volume designs will be on FPGAs (crossover point increases every year)
- FPGAs are useful even for ASIC design teams (rapid prototyping)
- FPGAs reduces design risk (avoid missing market window, accommodate bugs, changing standards, prolong lifetime of product)