CEG5010 Reconfigurable Computing

FPGA Architecture

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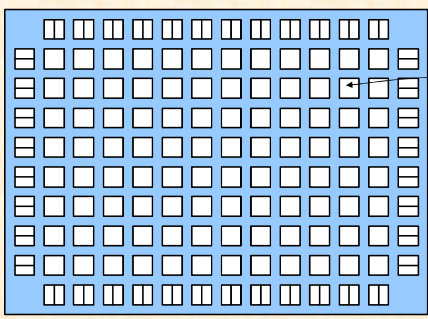
Introduction

- Architecture of an "Island-style" FPGA and how CAD tools map to them
- How to determine values for architectural parameters

Island-style FPGA – Logic Block

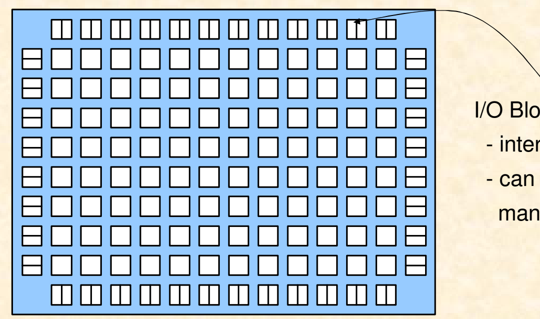


Logic Blocks
- used to implement logic
- lookup tables & flip-flops

Altera: LABs
Xilinx: CLBs

Slide: Steve Wilton, UBC

Island-style FPGA – I/O Block



I/O Blocks
- interface off-chip
- can usually support many I/O Standards

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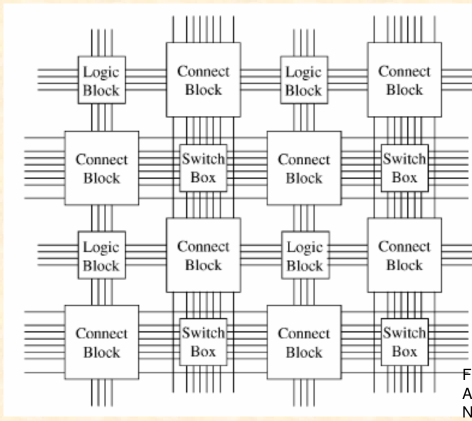
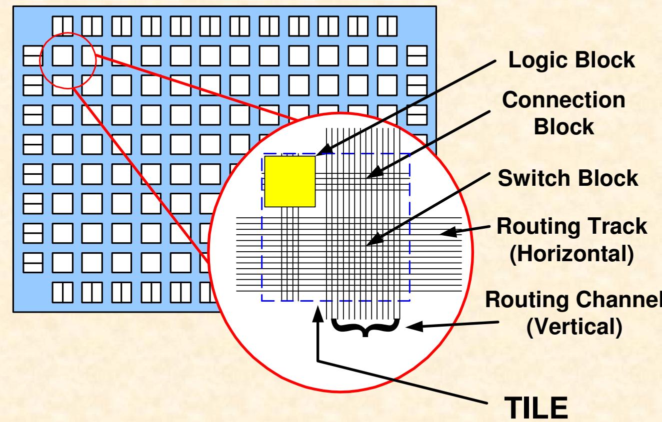
FPGA Blocks



From Compton & Hauck, ACM Comput. Surv., V34, No. 2, June 2002

Tile



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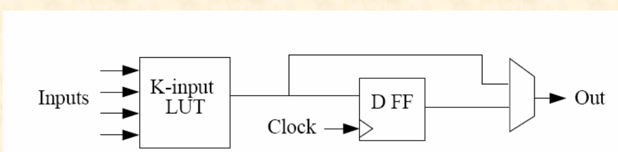
Basic Logic Element

- The lookup table size is K
  - What are the consequences of this being too big/small?

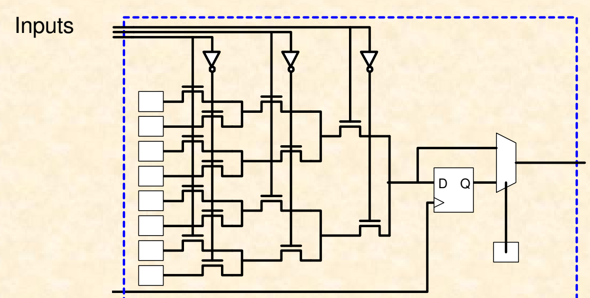


(a) Basic logic element (BLE)

From [1]

BLE Implementation

Basic Logic Gate: Lookup-Table



Function of each lookup table can be configured by shifting in bit-stream.

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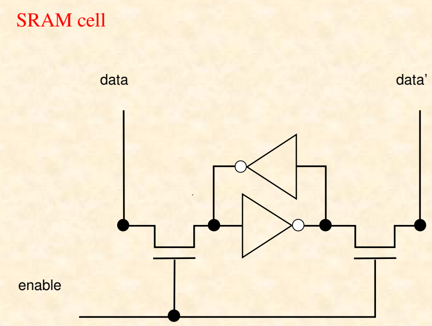
Exercise

- Show how we can implement A+B+(C.D) with the LUT in the previous slide
- How many of the following does a K-input LUT use?
  - SRAM cells
  - MUX pass transistors
  - MUX select buffers?

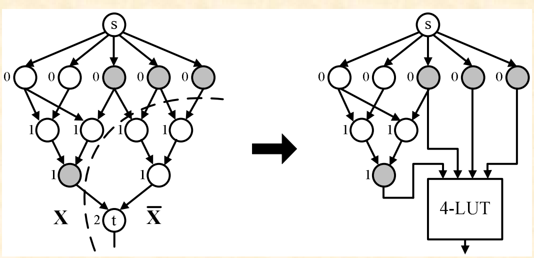
SRAM Cell



- How many transistors?

Technology Mapping

- Mapping gates to LUTs:



- Depth-optimal mapping

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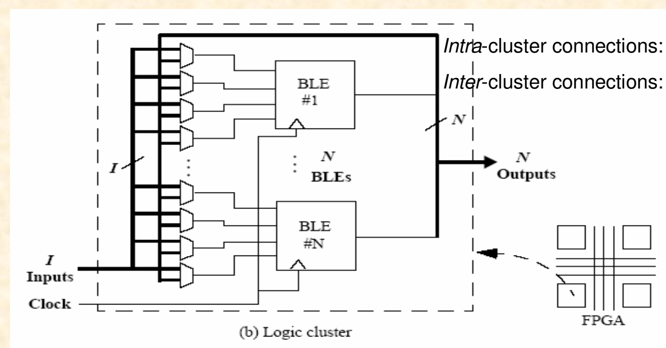
Logic Cluster

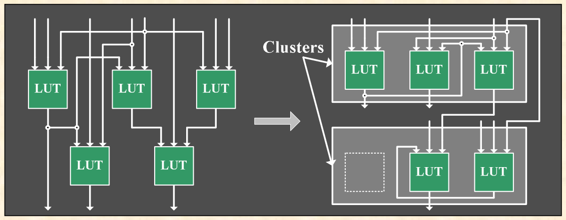


Cluster accepts I inputs and consists of N basic logic elements with multiplexed inputs

From [1]

Clustering Algorithms

- FPGA logic blocks (LABs, CLB's) usually contain several LUTs:



- Clustering groups LUTs into LAB-sized clusters
- - Idea: try to encapsulate as much activity inside each cluster as
- possible

Configurable Routing

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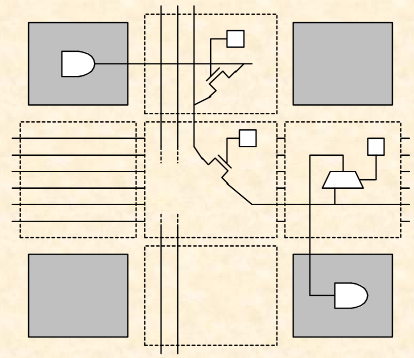
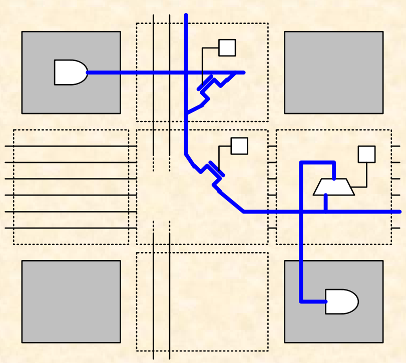


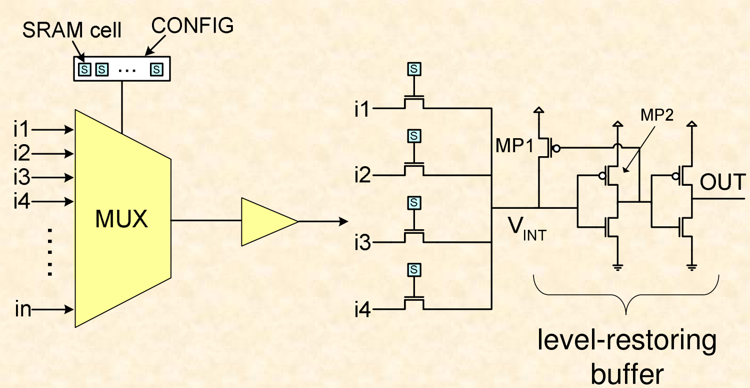
Connect Logic Blocks using Fixed Metal Tracks and Programmable Switches

Configurable Routing



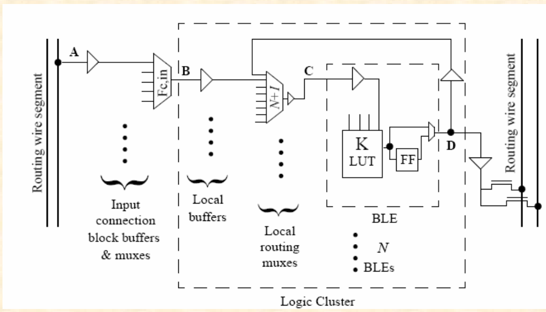
Connect Logic Blocks using Fixed Metal Tracks and Programmable Switches

Routing Switch



Logic Cluster Detail

- Fc,in is the number of input connections from routing to cluster

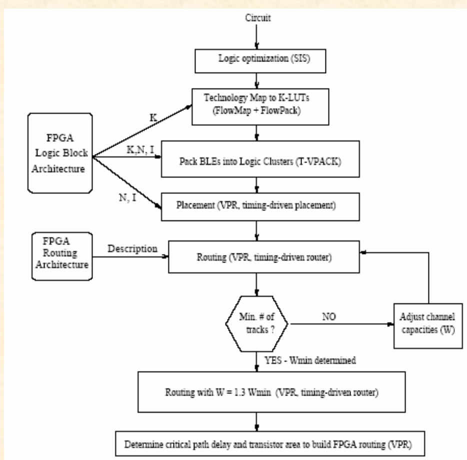


From [1]

Architectural Evaluation

- What value of I should we choose so 98% of LUTs in a cluster can be used?
- What is the effect of K and N on area and delay?
- These questions are circuit-specific so they involve an interaction of CAD tools with the architecture

Architectural Evaluation



From [1]

Delay

- Spice simulations used to characterize cluster and routing delays
- Timing model in VPR updated

MCNC Benchmarks

Circuit	# of 4-Input BLEs	# of Nets
alu4	1522	1536
apex2	1878	1916
apex4	1262	1271
bigkey	1707	1936
clma	8383	8445
des	1591	1847
diffeq	1497	1561
dsip	1370	1599
elliptic	3604	3735
ex1010	4598	4608
ex5p	1064	1072
frisc	3556	3576
misex3	1397	1411
pdc	4575	4591
s298	1931	1935
s38417	6406	6435
s38584.1	6447	6485
seq	1750	1791
spla	3690	3706
tseng	1047	1099
display_chip	1794	2419
img_calc	10141	10180
img_interp	2727	2769
input_chip	807	841
peak_chip	809	840
scale125_chip	2632	2654
scale2_chip	1189	1202
warping	1353	1394

I required for 98% Utilization

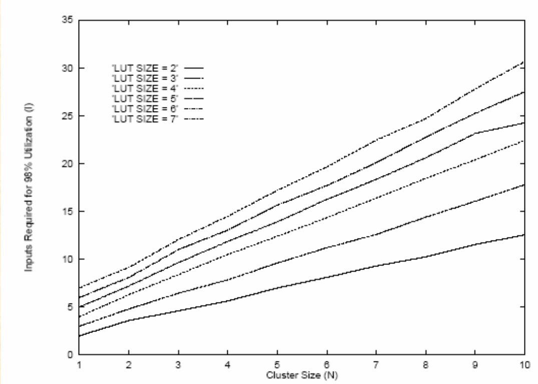
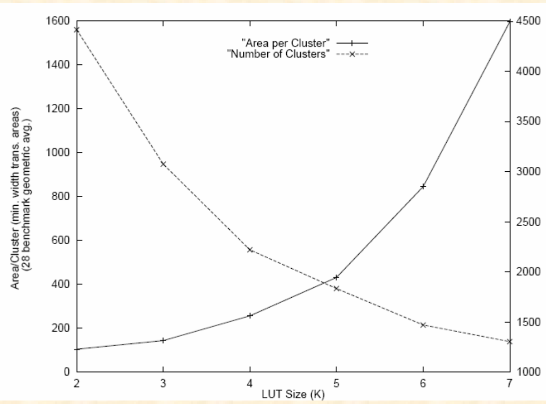


Fig. 6. Number of Inputs Required for 98% Logic Block Utilization

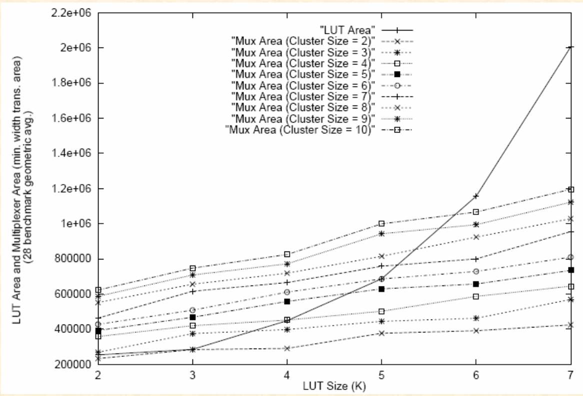
Empirical relationship: $I = \frac{K}{2}(N+1)$

Area vs N and K



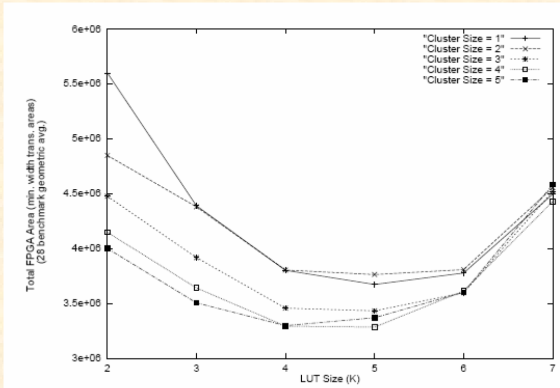
Number of clusters reduced as K increases but area increased

Breakdown of area usage

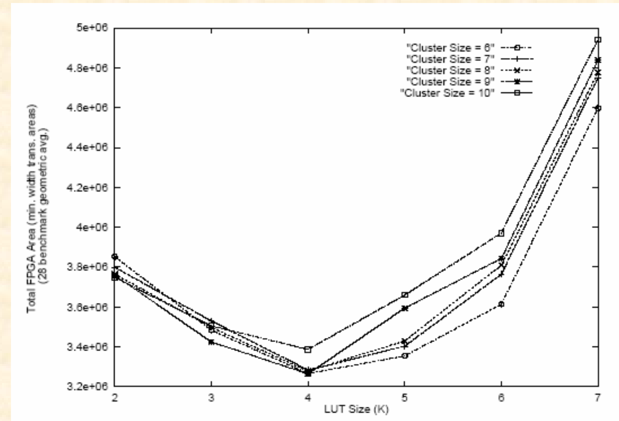


- Intra-cluster mux area significant for large cluster size

Area vs N and K



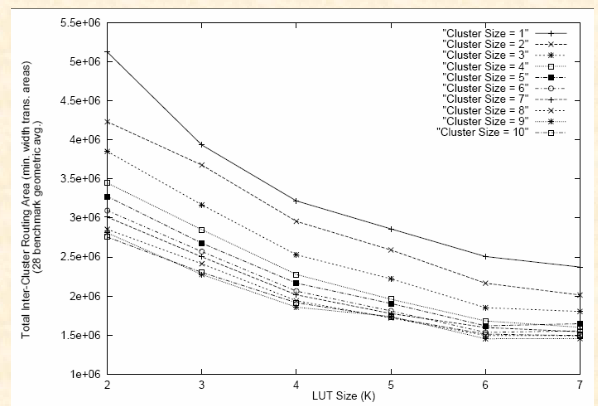
Area vs N and K



Area vs N and K

- Area measure is geometric average of total area of all benchmarks
- LUTs of size 4-5 are most area efficient
- Reduction in area as cluster size increased from 1 to 3 for all LUT sizes. For N>4, little impact on total area

Inter-cluster routing area

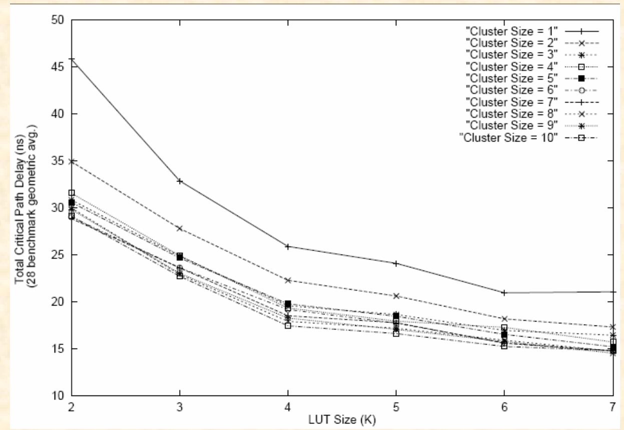


- Decreases linearly with K

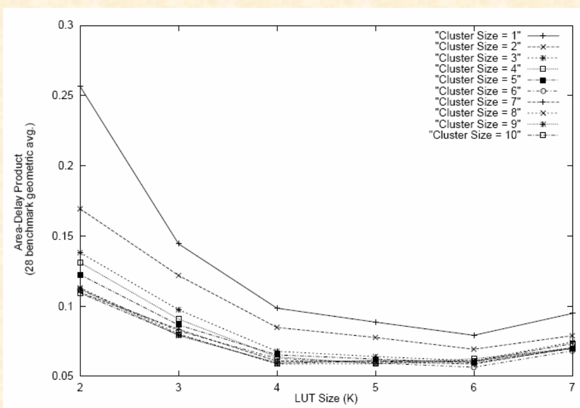
Delay vs Cluster Size

- As LUT and cluster size increases
  - delay through a cluster increases
  - number of LUTs and clusters in series on critical path decreases

Delay vs Cluster Size



Area-delay product



LUTs size 4-6 and cluster size 3 to 10 best

Summary

- Introduced island style FPGA architecture
- [1] describes a methodology for evaluating the impact of different architectural parameters on area, delay, area*delay
- Remember that the results are also a function of IC technology, CAD tools and benchmarks

References

[1] Elias Ahmed, Jonathan Rose: The effect of LUT and cluster size on deep-submicron FPGA performance and density. IEEE Trans. VLSI Syst. 12(3): 288-298 (2004)

Review Exercises

- What is K and N for the Virtex-5 and Stratix-III architectures?
- How many LUTs does it take to implement a full adder?
- How is I related to K and N?
- How does K&N affect LUT area?
- Would changing the benchmarks change the results of this study?