

# CEG3470 Digital Circuits 2007

## Midterm Examination

### Equation Summary

#### Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

#### MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad (sat)$$

$$I_D = v_{sat} C_{ox} W \left( V_{GS} - V_T - \frac{V_{DSAT}}{2} \right) (1 + \lambda V_{DS}) \quad (velocitysat)$$

$$I_D = k'_n \frac{W}{L} \left( (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (triode)$$

$$I_D = I_S e^{\frac{V_{GS}}{n k T/q}} \left( 1 - e^{-\frac{V_{DS}}{k T/q}} \right) \quad (subthreshold)$$

#### Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L} \left( V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

with  $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$   
and  $V_{GT} = V_{GS} - V_T$

#### MOS Switch Model

$$R_{eq} = \frac{1}{2} \left( \frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right)$$

$$\approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left( 1 - \frac{5}{6} \lambda V_{DD} \right)$$

### Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L (V_{swing}/2)}{I_{avg}}$$

$$t_{pLH} = \sqrt{t_{pLH(step)}^2 + (t_f/2)^2}$$

$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

### Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M = \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2})}{1 + r}$$

$$\approx \frac{r V_{DD}}{1 + r} \text{ with } r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with  $g \approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left( \frac{R_{eqn} + R_{eqp}}{2} \right)$$

$$P_{av} = C_L V_{DD}^2 f$$

### Interconnect

Lumped RC:  $t_p = 0.69 RC$

Distributed RC:  $t_p = 0.38 RC$

$$RC\text{-chain: } \tau_N = \sum_{i=1}^N R_i \sum_{j=i}^N C_j = \sum_{i=1}^N C_i \sum_{j=1}^i R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_0}$$

In all answers, please show full working and intermediate results.

1. (a) (5 marks) In what situation does a lumped interconnect model give inaccurate results compared with a distributed model?
- (b) (10 marks) For the circuit in Figure 1, calculate its Elmore time constant. Hint, recall that  $R_{ik} = \sum R_j \implies (R_j \in [\text{path}(s \rightarrow i) \cap \text{path}(s \rightarrow k)])$  and  $\tau_{D_i} = \sum_{k=1}^N C_k R_{ik}$ .

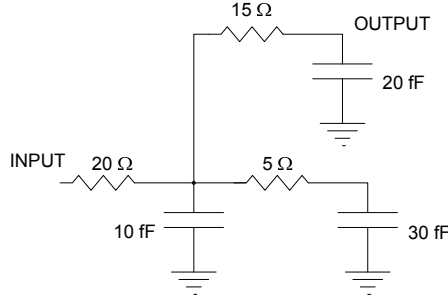


Figure 1: An RC circuit.

- (c) (10 marks) A chain of  $N$  identical RC elements is shown in Figure 2. Derive a simplified expression for the Elmore delay of this circuit.

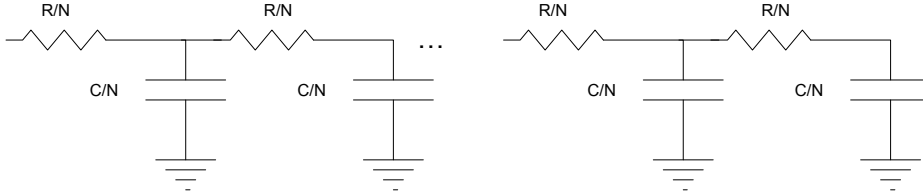


Figure 2: An RC transmission chain.

2. A minimum sized symmetric CMOS inverter is built from transistors having the following parameters  $V_{DD} = 2.5V$ ,  $W_N = 0.375\mu m$ ,  $L_N = 0.25\mu m$ ,  $V_{T0N} = 0.43V$ ,  $\gamma_N = 0.4V^{0.5}$ ,  $V_{DSATN} = 0.63V$ ,  $K'_N = 115 \times 10^{-6} A/V^2$ ,  $\lambda_N = 0.06V^{-1}$ ,  $W_P = 1.125\mu m$ ,  $L_P = 0.25\mu m$ ,  $V_{T0P} = -0.4V$ ,  $\gamma_P = -0.4V^{0.5}$ ,  $V_{DSATP} = -1V$ ,  $K'_P = -30 \times 10^{-6} A/V^2$ ,  $\lambda_P = -0.1V^{-1}$ . The inverter is attached to a 3 fF load.
  - (a) (10 marks) What is the output low voltage ( $V_{OL}$ ), input low voltage ( $V_{IL}$ ) and noise margin low ( $NM_L$ ) for this inverter?
  - (b) (10 marks) What is the high to low propagation delay ( $t_{pHL}$ ) for this inverter?
  - (c) (5 marks) Assuming that the inverter is being driven by an input with 10 ps rise/fall time instead of a step input, what will be the worse case high to low propagation delay?

3. (a) (5 marks) Draw a cross section view of a PMOS transistor. On your diagram label the P+, oxide, poly, Nwell and Pwell regions.
- (b) (5 marks) Explain why sub-threshold conduction is becoming more of a problem in modern integrated circuits.
- (c) (5 marks) An NMOS transistor has the following parameters:  $V_{DD} = 2.5\text{ V}$ ,  $W_N = 0.5\ \mu\text{m}$ ,  $L_N = 0.25\ \mu\text{m}$ ,  $V_{T0N} = 0.5\text{ V}$ ,  $\gamma_N = 0.4\text{ V}^{0.5}$ ,  $V_{DSATN} = 0.6\text{ V}$ ,  $K'_N = 100 \times 10^{-6}\text{ A/V}^2$  and  $\lambda_N = 0\text{ V}^{-1}$ . What is the maximum current that this transistor can deliver?
- (d) (10 marks) Due to process variations, the  $W_N$ ,  $L_N$  and  $V_{T0N}$  of the transistor in Question 4c can vary by  $\pm 10\%$ . What guaranteed maximum current can be specified?
4. (a) (5 marks) Explain whether (a) an inverter with slow input, fast output or (b) an inverter with fast input, slow output has a lower short-circuit current.
- (b) (10 marks) An inverter buffer is inserted to drive a 3 pF load from a minimum sized inverter ( $C_i = 10\text{ fF}$ ) as shown in Figure 3. What is the minimum propagation delay that can be achieved? Assume that the intrinsic delay,  $t_{p0}$  of the minimum sized inverter is 50 ps,  $\gamma = 1$  and  $t_p = t_{p0}(1 + \frac{C_{ext}}{\gamma C_g})$ .

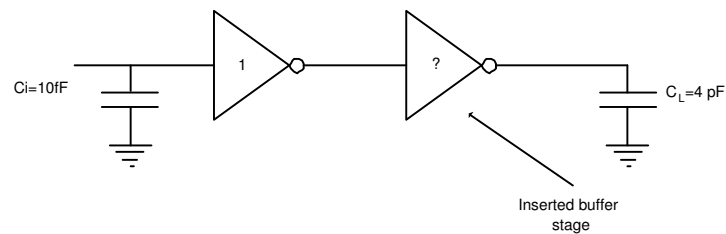


Figure 3: A buffer circuit.

- (c) (10 marks) Calculate the energy consumption of the entire buffer circuit, taking into account the input and output capacitance of the buffers. Hint: use  $C_{int} = \gamma C_g$ .

1. (a) A lumped model assumes that the potential of all points along a wire are the same. A distributed model should be used when the rise/fall time of the input is smaller than the rise/fall of the line i.e.  $t_{rise} < RC$ . For example, treating a fast signal with  $t_r = 100 ps$  feeding into a long wire with  $RC = 1 ns$  as a lumped system will lead to inaccurate estimates of propagation delay.

(b)

$$\tau = C_1 R_{i1} + C_2 R_{i2} + C_3 R_{i3} \quad (1)$$

$$= C_1 R_1 + C_2 (R_1) + C_i (R_1 + R_i) \quad (2)$$

$$= 10 \times 20 + 30 \times 20 + 20(20 + 15) fs \quad (3)$$

$$= 200 + 600 + 700 fs \quad (4)$$

$$= 1.5 ps \quad (5)$$

(c)

$$\tau = C_1 R_1 + C_2 (R_1 + R_2) + \dots + C_i (R_1 + R_2 + \dots R_1) \quad (6)$$

$$= \frac{C}{N} \left( \frac{R}{N} + \frac{2R}{N} + \dots + \frac{NR}{N} \right) \quad (7)$$

$$= \frac{C}{N} \frac{R}{N} \left( \frac{N(N+1)}{2} \right) \quad (8)$$

$$= \frac{RC}{N} \left( \frac{N+1}{2} \right) \quad (9)$$

2. (a)

$$V_{OL} = 0 V \quad (10)$$

$$r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} \quad (11)$$

$$= \frac{1.125/0.25 * 30e-6}{0.375/0.25 * 115e-6} \quad (12)$$

$$= 0.783 \quad (13)$$

$$V_m = \frac{0.43 + 0.63/2 + r(2.5 - 0.4 - 0.5)}{1 + r} \quad (14)$$

$$= 1.12 V \quad (15)$$

$$g \approx -\frac{1 + r}{(1.12 - 0.43 - 0.63/2) * (0.06 + 0.1)} \quad (16)$$

$$= -29.7 \quad (17)$$

$$V_{IL} = 1.12 + \frac{2.5 - 1.12}{-29.7} \quad (18)$$

$$= 1.073 \quad (19)$$

$$NM_L = V_{IL} \quad (20)$$

$$= 1.073 V \quad (21)$$

(b)

$$I_D = \frac{0.375}{0.25} * 115e-6 - ((2.5 - 0.43) * 0.63 - 0.63^2/2)(1 + 0.06 * 2.5) \quad (22)$$

$$= 219e-6 A \quad (23)$$

$$R_{eq} \approx 0.75 * \frac{2.5}{I_D} (1 - 5/6 * 0.06 * 2.5) \quad (24)$$

$$= 8.7 k \quad (25)$$

$$t_{pHL} = 0.69 * 8.7e3 * 3e-15 \quad (26)$$

$$= 18 ps \quad (27)$$

$$(c) \sqrt{18^2 + (10/2)^2} = 18.7 \text{ ps}$$

3. (a) Refer to textbook.  
 (b) Leakage of cutoff transistors causes static power consumption that becomes large if there are a lot of transistors.  
 (c)  $2 * 100e - 6 * ((2.5 - 0.5) * 0.6 - 0.6^2/2) = 204e - 6 \text{ A}$   
 (d)  $\frac{0.9 * 0.5}{1.1 * 2.5} * 100e - 6 * ((2.5 - (1.1 * 0.5)) * 0.6 - 0.6^2/2) = 162e - 6 \text{ A}$
4. (a) Fast input has a lower short circuit input current as the transistor is cutoff most of the time  
 (b)  $f = \sqrt{3e - 12/10e - 15} = 17.3$  so  $t = 2 * 50(1 + f/\gamma) = 1.83 \text{ ns}$ .  
 (c)  $E = V_{dd}^2 * C_g((1 + \gamma)(1 + f) + F) = 2.5^2 * 10e - 15 * (2 * 18.3 + 300) = 21 \text{ nJ}$