CEG3470 Digital Circuits 2004
Midterm Examination

Equation Summary

Diode

$$
\begin{aligned}
I_D &= I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T \\
C_j &= \frac{C_{j0}}{(1 - V_D/\phi_0)^m} \\
K_{eq} &= \frac{-\phi_0^m}{(V_{high} - V_{low})(1-m)} \times \\
&\quad [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]
\end{aligned}
$$

MOS Transistor

$$
\begin{aligned}
V_T &= V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|}) \\
I_D &= \frac{k'_n}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad (sat) \\
I_D &= v_{sat}C_{ox}W\left(V_{GS} - V_T - \frac{V_{DSAT}}{2}\right)(1 + \lambda V_{DS}) \\
&\quad (velocitysat) \\
I_D &= k'_n\frac{W}{L}\left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right) \quad (triode) \\
I_D &= I_S e^{\frac{V_{GS}}{nkT/q}}\left(1 - e^{-\frac{V_{DS}}{kT/q}}\right) \quad (subthreshold)
\end{aligned}
$$

Deep Submicron MOS Unified Model

$$
\begin{aligned}
I_D &= 0 \; for \; V_{GT} \leq 0 \\
I_D &= k'\frac{W}{L}\left(V_{GT}V_{min} - \frac{V_{min}^2}{2}\right)(1 + \lambda V_{GS}) \; for \; V_{GT} \geq 0
\end{aligned}
$$

$with \; V_{min} = min(V_{GT}, V_{DS}, V_{DSAT})$

$and \; V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$
\begin{aligned}
R_{eq} &= \frac{1}{2}\left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)}\right) \\
&\approx \frac{3}{4}\frac{V_{DD}}{I_{DSAT}}\left(1 - \frac{5}{6}\lambda V_{DD}\right)
\end{aligned}
$$

Inverter

$$
\begin{aligned}
V_{OH} &= f(V_{OL}) \\
V_{OL} &= f(V_{OH}) \\
V_M &= f(V_M) \\
t_p &= 0.69R_{eq}C_L = \frac{C_L(V_{swing}/2)}{I_{avg}} \\
t_{pLH} &= \sqrt{t_{pLH(step)}^2 + (t_f/2)^2} \\
t_{pHL} &= \sqrt{t_{pHL(step)}^2 + (t_r/2)^2} \\
P_{dyn} &= C_L V_{DD} V_{swing} f \\
P_{stat} &= V_{DD} I_{DD}
\end{aligned}
$$

Static CMOS Inverter

$$
\begin{aligned}
V_{OH} &= V_{DD} \\
V_{OL} &= GND \\
V_M &= \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2})}{1 + r} \\
&\approx \frac{rV_{DD}}{1 + r} \; with \; r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} \\
V_{IH} &= V_M - \frac{V_M}{g} \qquad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}
\end{aligned}
$$

$$with \; g \approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

$$
\begin{aligned}
t_p &= \frac{t_{pHL} + t_{pLH}}{2} = 0.69C_L\left(\frac{R_{eqn} + R_{eqp}}{2}\right) \\
P_{av} &= C_L V_{DD}^2 f
\end{aligned}
$$

Interconnect

Lumped RC: $t_p = 0.69RC$

Distributed RC: $t_p = 0.38RC$

RC-chain: $\tau_N = \sum_{i=1}^{N} R_i \sum_{j=i}^{N} C_j = \sum_{i=1}^{N} C_i \sum_{j=1}^{i} R_j$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_o}$$

In all answers, please show full working and intermediate results.

1. (a) (5 marks) What is channel length modulation and how is it modeled in the MOS transistor equations?
   (b) (5 marks) Explain the relationship between the equivalent resistance of a MOS transistor and its (W/L) ratio.
   (c) (5 marks) Explain using a diagram why the gate to bulk capacitance of a MOS transistor becomes zero in the resistive region of operation.
   (d) (5 marks) Give one advantage and one disadvantage associated with reducing the threshold voltage in an IC process.
   (e) (5 marks) How is the speed of a MOS transistor affected by reducing the thickness of the gate oxide? Explain your answer.

2. (a) (5 marks) What advantages does copper interconnect provide compared with aluminium?
   (b) (10 marks) Draw a cross section view of a PMOS transistor. On your diagram show the N+, P+, oxide, poly, Nwell and Pwell regions and identify the gate, source, drain and bulk connections of the transistor.
   (c) (10 marks) Estimate the propagation delay of a signal along a 5 mm track of metal1 material with $r = 0.08\ \Omega/\mu m$ and $c = 0.1\ fF/\mu m$. The signal is driven by a signal generator with source resistance of 1 $k\Omega$. Use a distributed rather than a lumped model for your working.

3. A minimum sized symmetric CMOS inverter is built from transistors having the following parameters $V_{DD} = 2.5V$, $W_N = 0.375\mu m$, $L_N = 0.25\mu m$, $VT0_N = 0.43V$, $\gamma_N = 0.4V^{0.5}$, $VDSAT_N = 0.63V$, $K'_N = 115 \times 10^{-6} A/V^2$, $\lambda_N = 0.06V^{-1}$, $W_P = 1.125\mu m$, $L_P = 0.25\mu m$, $VT0_P = -0.4V$, $\gamma_P = -0.4V^{0.5}$, $VDSAT_P = -1V$, $K'_P = -30 \times 10^{-6} A/V^2$, $\lambda_P = -0.1V^{-1}$. The inverter is attached to a 5 fF load.
   (a) (10 marks) What should the value of W_P be changed to if we would like the switching threshold (V_M) to be 1 V? Use the equation $V_M = \frac{(V_{Tn}+\frac{V_{DSATn}}{2})+r(V_{DD}+V_{Tp}+\frac{V_{DSATp}}{2})}{1+r}$ where $r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$ in your working.
   (b) (10 marks) What is the current flowing through the NMOS transistor during a high-to-low transition (assume a step input) when the output voltage is 2.5 V and 1.25 V respectively. Include channel length modulation effects in your answer.
   (c) (5 marks) Assuming that the inverter is being driven by an input with 50ps rise/fall time instead of a step input, what will be the worse case high to low propagation delay?

4. (a) (10 marks) An inverter buffer is inserted to drive a 4 pF load from a minimum sized inverter ($C_i = 10\ fF$) as shown in Figure 1. What is the most appropriate sizing of the inverter to minimize the propagation delay and what is the resulting propagation delay? Assume that the intrinsic delay, t_{p0} of the minimum sized inverter is 50 ps, $\gamma = 1$ and $t_p = t_{p0}(1 + \frac{C_{ext}}{\gamma C_g})$.

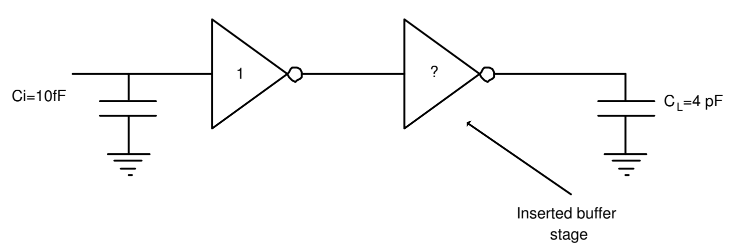

Figure 1: A buffer circuit.

   (b) (10 marks) What is the optimal propagation delay if 4 arbitrary size inverters are allowed?
   (c) (5 marks) Would 4 inverters be a good choice for $\gamma = 0$? Explain your answer.