

Course Examinations 2004-2005

Course Code & Title : CEG 3470 Digital Circuits

Time allowed : 2 hours 0 minutes

Student I.D. No. : Seat No. :

Equation Summary

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n W}{2 L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) \quad (sat)$$

$$I_D = v_{sat} C_{ox} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right) (1 + \lambda V_{DS}) \quad (velocitysat)$$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (triode)$$

$$I_D = I_S e^{\frac{V_{GS}}{nkT/q}} \left(1 - e^{-\frac{V_{DS}}{kT/q}} \right) \quad (subthreshold)$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L} \left(V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{DS}) \text{ for } V_{GT} \geq 0$$

$$\text{with } V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$$

$$\text{and } V_{GT} = V_{GS} - V_T$$

MOS Switch Model

$$R_{eq} = \frac{1}{2} \left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right) \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD} \right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L (V_{swing}/2)}{I_{avg}}$$

$$t_{pLH} = \sqrt{t_{pLH(step)}^2 + (t_f/2)^2}$$

$$t_{pHL} = \sqrt{t_{pHL(step)}^2 + (t_r/2)^2}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M = \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2})}{1 + r}$$

$$\text{with } r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

$$\text{with } g \approx \frac{1 + r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 C_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

$$\text{Lumped RC: } t_p = 0.69 RC$$

$$\text{Distributed RC: } t_p = 0.38 RC$$

$$\text{RC-chain: } \tau_N = \sum_{i=1}^N R_i \sum_{j=i}^N C_j = \sum_{i=1}^N C_i \sum_{j=1}^i R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_0}$$

In all answers, please show full working and intermediate results.

1. (a) (5 marks) Suppose a PMOS transistor is used to charge a load C_L from 0 V to V_{DD} . What would be the effect on the energy consumption of this circuit if the width W of the transistor were doubled?
 - (b) (5 marks) Explain the relationship between the equivalent resistance of a MOS transistor and its (W/L) ratio.
 - (c) (5 marks) Suppose we fabricate three transistors. Transistor A has dimensions $W = L = 0.25\mu m$, B has dimensions $W = L = 0.5\mu m$, and transistor C has $W = L = 25\mu m$. We then measure their drain current, I_{DS} with $V_{DS} = V_{GS} = V_{DD}$. Will their drain currents be different? Explain your answer.
 - (d) (5 marks) Give a reason why PMOS transistors are typically made larger than NMOS transistors in a CMOS inverter.
 - (e) (5 marks) Explain how velocity saturation is handled in the unified MOS transistor model.
2. Consider a complementary CMOS inverter with the following parameters: $V_{DD} = 2.5V$, $W_N = 0.375\mu m$, $L_N = 0.25\mu m$, $VT0_N = 0.43V$, $\gamma_N = 0.4V^{0.5}$, $V_{DSAT_N} = 0.63V$, $K'_N = 115 \times 10^{-6} A/V^2$, $\lambda_N = 0.06V^{-1}$. $W_P = 0.75\mu m$, $L_P = 0.25\mu m$, $VT0_P = -0.4V$, $\gamma_P = -0.4V^{0.5}$, $V_{DSAT_P} = -1V$, $K'_P = -30 \times 10^{-6} A/V^2$, $\lambda_P = -0.1V^{-1}$.

- (a) (5 marks) What is the switching threshold of this inverter?
- (b) (10 marks) Suppose that this inverter is driving a 1 pF load. Using the formula

$$R_{eq} \approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD} \right)$$

calculate the t_{pHL} of this inverter?

- (c) (10 marks) Suppose the inverter is connected to no load (i.e. $C_L = 0$). What is the maximum value of short circuit current, I_{SC} which will pass through the two transistors and at what input voltage level does it occur?
3. (a) (10 marks) Draw a static CMOS complementary gate which implements the function $f = \overline{A.(B + C)}$ (where $.$ is the logical AND function and $+$ is the logical OR function). Indicate the size of the NMOS and PMOS devices so that the output resistance is the same as that of an inverter with an NMOS $W/L=3$ and PMOS $W/L=6$.
- (b) (10 marks) Draw a domino logic implementation of a gate which implements the function $f = \overline{A.(B + C)}$.
 - (c) (5 marks) Using a diagram, explain how charge leakage affects the minimum operating frequency of a domino logic circuit.

Question 4 is on the next page

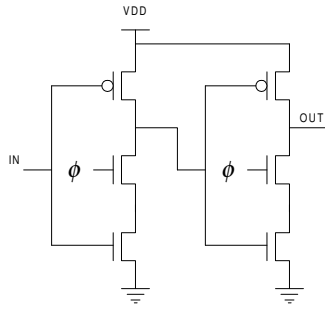


Figure 1: A true single phase clocked (TSPC) logic latch.

4. (a) (5 marks) Draw the schematic of a two stage, negative edge triggered dynamic shift register which only uses inverters and transmission gates. You can assume that non-overlapping clocks are available.
- (b) (10 marks) Explain why the true single phase clocked (TSPC) latch of Figure 1 can race if the slope of the clock is not fast enough.
- (c) (10 marks) Draw a transistor level schematic of a TSPC latch which computes the logical OR of two inputs A and B and latches the result.