

17-Feb-04 (1)

Using the FPGA Editor

17-Feb-04 (2)

Introduction

- This week we will have a part lecture/part tutorial on using the FPGA Editor
 - generate a design which cannot be represented in VHDL

17-Feb-04 (5)

VHDL base code cont'd

```

begin
  force1 <= '1';
  process(clk)
  begin
    if (clk'event and clk = '1') then
      q(3) <= q(2);
      q(2) <= q(1);
      q(1) <= q(0);
      q(0) <= (not(q(3) xor
q(2))) xor (q(2) and q(1) and q(0));
      din2 <= dout1;
      dout <= dout2;
    end if;
  end process;

  mem1 : ram16x1s port map
    ( D => din1, A0 => q(0),
      A1 => q(1), A2 => q(2),
      A3 => q(3), WE => force1,
      WCLK => clk, O => dout1);
  mem2 : ram16x1s port map
    ( D => din2, A0 => q(0),
      A1 => q(1), A2 => q(2),
      A3 => q(3), WE => force1,
      WCLK => clk, O => dout2);
end synthesis;

```

17-Feb-04 (6)

Modifications using EPIC

- Understand design
- Change pinout
- Swap component locations
- Remove nets, add nets
- Add components
- Modify designs

17-Feb-04 (7)

Things to do

- Trace a path using FPGA editor and the timing analyzer
- Swap CLBs and IOBs
- Change to use CLB FF instead of IOB

17-Feb-04 (8)

Conclusions

- Using EPIC we can directly view the resultant layout
 - understand the logic, placement and routing
 - make modifications to the design