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## CEG5010: Conclusion

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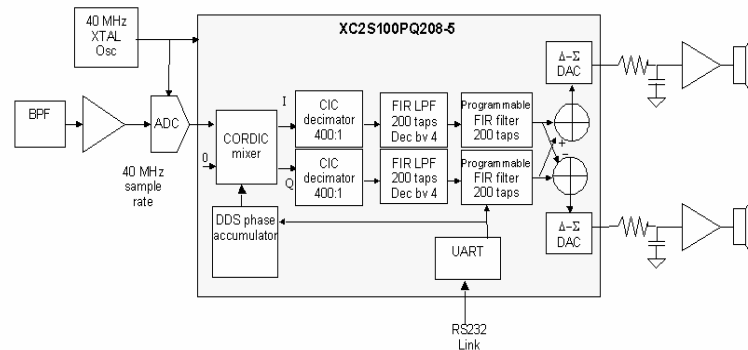
## What have we learnt?

- **FPGA**
  - When to use them
    - Low volume, upgradability, easy re-engineering
  - How to take advantage of the architecture
    - Runtime reconfiguration
    - Use special features: RAM, SRL, DLL, flip-flop rich
- **Computer Arithmetic**
  - Bit/digit serial techniques
  - Distributed arithmetic
  - CORDIC
  - STAM
- **Computer Architecture**
  - Finding parallelism via pipelining and parallel processing
  - Customization for a given problem: module generators, runtime specialization
  - Bus interfaces can be a bottleneck

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## Example application where many of these ideas are used (Andraka software radio)

We'll be showing off a direct conversion shortwave receiver demo implemented on an insight SpartanII-100 eval board connected to a Burr Brown ADS807E A/D converter eval board on demo night (April 9th). The entire radio consists of these two boards, a pair of single pole RC filters driving a pair of PC speakers and an Ameco Tunable antenna preamp.



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## Demonstration

- Next week during double period
- Informal demo to give me a chance to ask questions about your project
  - Show understanding of the problem and design decisions made
  - Fill in “Project report sheet” at [http://www.cse.cuhk.edu.hk/~phwl/ceg5010/design/report\\_sheet.doc](http://www.cse.cuhk.edu.hk/~phwl/ceg5010/design/report_sheet.doc) before the demo

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## Assignment

- Due 7<sup>th</sup> May, 10% deducted per day late
- 4 page report include previous work, full description of system, system performance, resource utilization, memory map etc (like a full conference paper)
- Appendix: Host program, VHDL listing, simulation graphs
- Submit hardcopy to Brittle

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## Exam

- 2hr open note exam
- Bring your calculator, notes, papers and Xilinx Virtex data sheet
- 3 questions
  - (25 marks) General short questions
  - (25 marks) Distributed arithmetic question
  - (50 marks) A bit-parallel design (algorithm given, must draw datapath and control and then give VHDL description)