CEG5010: Conclusion

What have we learnt?

• FPGA
  – When to use them
    • Low volume, upgradability, easy re-engineering
  – How to take advantage of the architecture
    • Runtime reconfiguration
    • Use special features: RAM, SRL, DLL, flip-flop rich

• Computer Arithmetic
  – Bit/digit serial techniques
  – Distributed arithmetic
  – Cordic
  – STAM

• Computer Architecture
  – Finding parallelism via pipelining and parallel processing
  – Customization for a given problem: module generators, runtime specialization
  – Bus interfaces can be a bottleneck
Example application where many of these ideas are used (Andraka software radio)

Demonstration

- Next week during double period
- Informal demo to give me a chance to ask questions about your project
  - Show understanding of the problem and design decisions made
  - Fill in “Project report sheet” at http://www.cse.cuhk.edu.hk/~phwl/ceg5010/design/report_sheet.doc before the demo
Assignment

• Due 7th May, 10% deducted per day late
• 4 page report include previous work, full description of system, system performance, resource utilization, memory map etc (like a full conference paper)
• Appendix: Host program, VHDL listing, simulation graphs
• Submit hardcopy to Brittle

Exam

• 2hr open note exam
• Bring your calculator, notes, papers and Xilinx Virtex data sheet
• 3 questions
  – (25 marks) General short questions
  – (25 marks) Distributed arithmetic question
  – (50 marks) A bit-parallel design (algorithm given, must draw datapath and control and then give VHDL description)