(When) Will FPGAs Kill ASICs?

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FPGAs vs. ASICs

- Cost – the real story.
- Time to market
- Why choose ASICs?
- Where are FPGAs going?
Unit Cost Analysis

ASIC Costs
Start higher, but slope is flatter

FPGA Costs
For each technology advance, crossover volume moves higher
Cost: The exploding ASIC NRE

![Graph showing NRE and Mask Costs vs. Process Geometry (Micron)]

Source: Dataquest
Time to market is critical

- Potential profit if you come early to the market
- Long time to market is a cost
- What you get if you design with an ASIC and come late to the market

Missing the market window will wipe out all savings from development and production
COST: System Reconfigurability

Lack of reconfigurability is a huge opportunity cost of ASICs
FPGAs offer flexible life cycle management
Breakeven Cost: Just the facts

- Total cost
- Unit cost
- Time-to-market
- Re-spins & Inventory
- Volume K units
- ASIC
Time To Market: Design Cycle

ASIC

Spec | Design & verification | Silicon Prototype | System Integration | Production | First Ship

FPGA

Spec | Design and verification | System Integration | Production | First Ship

Freeze design

Iterations?

- ASIC Methodology is very unforgiving
- FPGA flexibility allows late design changes
Designing with ASICs

Timing Closure is a very serious problem in DSM
Designing with FPGAs

- DSM Effects
- Process issues

Verification is much simpler

Super fast compile times
~1M gates in < 1hr

Timing Closure is a much simpler problem in FPGAs
Why do people design ASICs?

- Cost/Volume
- Performance
- Density
- IP Libraries
Volume requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries

>50% of market is available today for FPGAs

Source: IMS 2000
Gate count requirement for ASICs

- Cost
- Density
- Performance
- IP Libraries

FPGAs can address very large part of the ASIC market today

Source: IMS 2000
Performance requirement for ASICs

<table>
<thead>
<tr>
<th>Cost</th>
<th>Density</th>
<th>Performance</th>
<th>IP Libraries</th>
</tr>
</thead>
<tbody>
<tr>
<td>53.9</td>
<td>38.5</td>
<td>10.8</td>
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FPGAs can address very large part of the ASIC market today

Source: IMS 2000
IP in FPGAs

5 Years ago FPGAs were only gates and routing ~25000 gates

Today, there are several system-level features. ~10,000,000 gates

The trend to add more IP in FPGAs continues
The Question is …

- The question is not if FPGAs will kill ASICs
  - Everyone understands the advantages of programmability

- The real question is “How can I get programmability in my system?”

- More IP on an FPGA or Programmability on an ASIC?
What is the future? You decide…

<table>
<thead>
<tr>
<th></th>
<th>More IP on FPGA</th>
<th>More Prog. On ASIC</th>
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</thead>
<tbody>
<tr>
<td><strong>Time-to-market</strong></td>
<td>Verification remains simple</td>
<td>Verification remains a problem</td>
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<tr>
<td></td>
<td>Timing closure is easier</td>
<td>Timing closure remains an issue</td>
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<tr>
<td><strong>Cost</strong></td>
<td>NRE is non-existent</td>
<td>NRE not reduced</td>
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<td></td>
<td>Extensive reconfigurability</td>
<td>Very limited reconfigurability</td>
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<td><strong>Design methodology/Software</strong></td>
<td>Simple methodology</td>
<td>Still a complex methodology</td>
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<td></td>
<td>Ease of use</td>
<td>Ease of use is still lacking</td>
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<td></td>
<td>Extremely fast SW runtimes</td>
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