CEG 5010: Reconfigurable Computing
Lecture 3: ASICs vs FPGAs

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ASIC NRE

Source: IBM
Cost of Technology vs Volume

- **Crossover volume increases with decreasing feature size**

Who can afford High-end ICs?

- ASICs becoming only for extreme designs, volume, speed, size, low power
- Design cost is another issue (1981: 100 designer months $\rightarrow$ ~$1M 2002: 30,000 designer months $\rightarrow$ ~$300M)

Source: ITRS'99
FPGAs offer shorter design cycle and later design changes

Source: Xilinx

Time to market

• Shorter development cycle associated with FPGAs allows faster time to market
• Reconfigurability allows for in-field upgrades, extending the life cycle of the product
• Missing window of opportunity is very costly
Why do people use ASICs

- Cost
- Density
- Performance
- IP Libraries

Volume requirement for ASICs

Source: Xilinx
Gate count requirement for ASICs

Source: Xilinx

Performance requirement for ASICs

Source: Xilinx
IP libraries

• Trend is to embed useful IP on the FPGA
  – uP, multipliers, transceivers, DLLs, RAM, IO standards, DDR, impedance control

• IP/Core libraries
  – Implemented on the FPGA core e.g. FFT, PCI express, DDR ram controllers etc

• Domain-specific languages e.g. System Generator translates between MATLAB/Simulink and FPGA circuits

IP Libraries: Xilinx Example

• Xilinx Virtex II Pro
• PowerPC based
  – 420 Dhrystone MIPS at 300 MHz
  – 1 to 4 PowerPCs
  – 4 to 16 gigabit transceivers
  – 12 to 216 multipliers
  – 3,000 to 50,000 logic cells
  – 200k to 4M bits RAM
  – 204 to 852 I/O
  – $100-$500 (>25,000 units)

Up to 16 serial transceivers
• 822 Mbps to 3.125 Gbps

Courtesy of Xilinx
IP Libraries: Altera Example

- Altera’s Excalibur EPXA 10
- ARM (922T) hard core
- ~200 Dhrystone MIPS at ~200 MHz
- Devices range from ~200k to ~2 million programmable logic gates

Example: DSP (2002)

<table>
<thead>
<tr>
<th>Function</th>
<th>Industry’s Fastest DSP Processor Core</th>
<th>Virtex-II</th>
</tr>
</thead>
<tbody>
<tr>
<td>8 x 8 Multiply Accumulate</td>
<td>8.8 Billion NACs/s</td>
<td>0.5 Tera NACs/s</td>
</tr>
<tr>
<td>FIR Filter 256-tap Linear phase, 16-bit data/coefficients</td>
<td>1.1 GHz</td>
<td>160 MSPS</td>
</tr>
<tr>
<td>FFT 1024 point, 16-bit data</td>
<td>7.7 μs, 800 MHz</td>
<td>&lt; 1 μs, 140 MHz</td>
</tr>
</tbody>
</table>

Source: Xilinx
FPGA Area Efficiency

- FPGAs use more transistors
  - Does not mean higher yield any more because die are becoming pad limited (can't pack more die on a wafer)
  - We have more transistors than we can (afford to) design anyway
- FPGAs about 10x area and 3x slower than ASICs – is this important?

Conclusions

- The prohibitive costs of advanced IC technology means more and more low-medium volume designs will be on FPGAs (crossover point increases every year)
- FPGAs are useful even for ASIC design teams (rapid prototyping)
- FPGAs reduces design risk (avoid missing market window, accommodate bugs, changing standards, prolong lifetime of product)