

CEG3470 Digital Circuits 2003

Midterm Examination

Equation Summary

Diode

$$I_D = I_S(e^{V_D/\phi_T} - 1) = Q_D/\tau_T$$

$$C_j = \frac{C_{j0}}{(1 - V_D/\phi_0)^m}$$

$$K_{eq} = \frac{-\phi_0^m}{(V_{high} - V_{low})(1 - m)} \times [(\phi_0 - V_{high})^{1-m} - (\phi_0 - V_{low})^{1-m}]$$

MOS Transistor

$$V_T = V_{T0} + \gamma(\sqrt{|-2\phi_F + V_{SB}|} - \sqrt{|-2\phi_F|})$$

$$I_D = \frac{k'_n W}{2L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \quad (sat)$$

$$I_D = v_{sat} C_{ox} W \left(V_{GS} - V_T - \frac{V_{DSAT}}{2} \right) (1 + \lambda V_{DS}) \quad (velocitysat)$$

$$I_D = k'_n \frac{W}{L} \left((V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2} \right) \quad (triode)$$

$$I_D = I_S e^{\frac{V_{GS}}{n k T/q}} \left(1 - e^{-\frac{V_{DS}}{k T/q}} \right) \quad (subthreshold)$$

Deep Submicron MOS Unified Model

$$I_D = 0 \text{ for } V_{GT} \leq 0$$

$$I_D = k' \frac{W}{L} \left(V_{GT} V_{min} - \frac{V_{min}^2}{2} \right) (1 + \lambda V_{GS}) \text{ for } V_{GT} \geq 0$$

with $V_{min} = \min(V_{GT}, V_{DS}, V_{DSAT})$
and $V_{GT} = V_{GS} - V_T$

MOS Switch Model

$$R_{eq} = \frac{1}{2} \left(\frac{V_{DD}}{I_{DSAT}(1 + \lambda V_{DD})} + \frac{V_{DD}/2}{I_{DSAT}(1 + \lambda V_{DD}/2)} \right)$$

$$\approx \frac{3}{4} \frac{V_{DD}}{I_{DSAT}} \left(1 - \frac{5}{6} \lambda V_{DD} \right)$$

Inverter

$$V_{OH} = f(V_{OL})$$

$$V_{OL} = f(V_{OH})$$

$$V_M = f(V_M)$$

$$t_p = 0.69 R_{eq} C_L = \frac{C_L (V_{swing}/2)}{I_{avg}}$$

$$P_{dyn} = C_L V_{DD} V_{swing} f$$

$$P_{stat} = V_{DD} I_{DD}$$

Static CMOS Inverter

$$V_{OH} = V_{DD}$$

$$V_{OL} = GND$$

$$V_M \approx \frac{r V_{DD}}{1+r} \text{ with } r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$$

$$V_{IH} = V_M - \frac{V_M}{g} \quad V_{IL} = V_M + \frac{V_{DD} - V_M}{g}$$

with $g \approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} = 0.69 RC_L \left(\frac{R_{eqn} + R_{eqp}}{2} \right)$$

$$P_{av} = C_L V_{DD}^2 f$$

Interconnect

Lumped RC: $t_p = 0.69RC$

Distributed RC: $t_p = 0.38RC$

$$RC\text{-chain: } \tau_N = \sum_{i=1}^N R_i \sum_{j=i}^N C_j = \sum_{i=1}^N C_i \sum_{j=1}^i R_j$$

Transmission line reflection:

$$\rho = \frac{V_{refl}}{V_{inc}} = \frac{I_{refl}}{I_{inc}} = \frac{R - Z_0}{R + Z_0}$$

In all answers, please show full working and intermediate results.

1. (a) (5 marks) Does increasing the length of a transistor reduce or increase the effects of velocity saturation? Explain why.
- (b) (5 marks) Explain why PMOS transistors have lower output current than an equivalent NMOS transistor.
- (c) (5 marks) Does energy consumption increase or decrease with supply voltage? How about delay?
- (d) (5 marks) Give two reasons why one might want to reduce the threshold voltage in an IC process.
- (e) (5 marks) Does the effect of channel length modulation increase or decrease with increasing transistor length?
2. (a) (5 marks) What advantages does copper interconnect provide compared with aluminium?
- (b) (10 marks) Show how one can construct a diode on an CMOS integrated circuit using a cross sectional view to explain your answer. On your diagram show which is the anode and cathode and clearly label the N+, P+, Nwell, Pwell and wiring regions.
- (c) (10 marks) Draw a cross section view of an inverter. On your diagram show the N+, P+, oxide, poly, Nwell and Pwell regions as well as how they are connected together (don't forget the well connections). Also label the VDD, GND, IN and OUT connections.
3. A minimum sized symmetric CMOS inverter is built from transistors having the following parameters $V_{DD} = 2.5V$, $W_N = 0.375\mu m$, $L_N = 0.25\mu m$, $V_{T0N} = 0.43V$, $\gamma_N = 0.4V^{0.5}$, $V_{DSATN} = 0.63V$, $K'_N = 115 \times 10^{-6} A/V^2$, $\lambda_N = 0.06V^{-1}$, $W_P = 1.125\mu m$, $L_P = 0.25\mu m$, $V_{T0P} = -0.4V$, $\gamma_P = -0.4V^{0.5}$, $V_{DSATP} = -1V$, $K'_P = -30 \times 10^{-6} A/V^2$, $\lambda_P = -0.1V^{-1}$. The inverter is attached to a 5 fF load.

In an integrated circuit, the threshold voltage can vary by $\pm 50 mV$ and the width and length of the transistor can vary by $\pm 10\%$ due to lithographic variations. Assuming that these are the main source of variation on the chip, what would be the:

- (a) (10 marks) Maximum switching threshold. Use the formula

$$V_M = \frac{(V_{Tn} + \frac{V_{DSATn}}{2}) + r(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2})}{1 + r}$$

where $r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}}$ to calculate the switching threshold.

- (b) (10 marks) Worst case high to low propagation delay (t_{PHL}) for a step input.
- (c) (5 marks) Assuming that the inverter is being driven by an input with 50ps rise/fall time instead of a step input, what will be the worst case high to low propagation delay?
4. (a) (5 marks) Draw a schematic of a complementary CMOS gate which implements the logical function $f(A,B,C)=\text{NOT}(A \text{ or } (B \text{ and } C))$.
- (b) (10 marks) Assuming that the length of both PMOS and NMOS transistors is fixed at $0.25\mu m$, suggest appropriate sizes for the transistors of the gate in the previous question so that worst case rise and fall times are approximately equal (assume $W_p = 2W_n$ achieves equal rise and fall times in the case of an inverter).
- (c) (10 marks) Draw a schematic of a pseudo-NMOS gate which implements the logical function $f(A,B,C)=\text{NOT}(A \text{ or } (B \text{ and } C))$. Derive a symbolic expression for the low to high propagation delay of your gate to a step input. The equation should be in terms of the variables C_L , V_{DD} , k' , W , L , V_T and V_{DSAT} .