

# Analysis of Digital Circuits

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## 1 Devices

### 1.1 MOS Transistor Summary

#### 1.1.1 NMOS

**Transconductance**

$$K_N = K'_N \frac{W}{L} = \mu_n C_{OX} \frac{W}{L} \quad (1)$$

**Threshold voltage**

$$V_{TN} = V_{T0} + \gamma(\sqrt{(V_{SB} + 2\phi_F)} - \sqrt{(2\phi_F)}) \quad (2)$$

**Cutoff**

$$I_{DS} = 0 \quad (V_{GS} \leq V_{TN}) \quad (3)$$

**Linear**

$$I_{DS} = K_N((V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}) \quad (V_{GS} - V_{TN} \geq V_{DS} \geq 0) \quad (4)$$

**Saturation**

$$I_{DS} = \frac{K_N}{2}(V_{GS} - V_{TN})^2 \quad (V_{DS} \geq V_{GS} - V_{TN} \geq 0) \quad (5)$$

#### 1.1.2 PMOS

**Transconductance**

$$K_P = K'_P \frac{W}{L} = \mu_p C_{OX} \frac{W}{L} \quad (6)$$

**Threshold voltage**

$$V_{TP} = V_{T0} - \gamma(\sqrt{(V_{BS} + 2\phi_F)} - \sqrt{(2\phi_F)}) \quad (7)$$

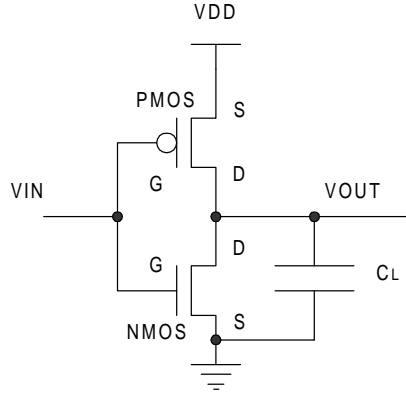


Figure 1: CMOS inverter.

### Cutoff

$$I_{SD} = 0 \quad (V_{SG} \leq -V_{TP}) \quad (8)$$

### Linear

$$I_{SD} = K_P \left( (V_{SG} + V_{TP}) V_{SD} - \frac{V_{SD}^2}{2} \right) \quad (V_{SG} + V_{TP} \geq V_{SD} \geq 0) \quad (9)$$

### Saturation

$$I_{SD} = \frac{K_P}{2} (V_{SG} + V_{TP})^2 \quad (V_{SD} \geq V_{SG} + V_{TP} \geq 0) \quad (10)$$

## 2 CMOS Inverter

The CMOS inverter is shown in Figure 1. In this configuration, from Kirchoff's voltage law, the following equations hold for the PMOS device

$$V_{SD} = V_{DD} - V_{OUT} \quad (11)$$

and

$$V_{SG} = V_{DD} - V_{IN}. \quad (12)$$

In addition, by Kirchoff's current law, the current in both transistors is the same

$$I_{DSN} = I_{SDP} \quad (13)$$

### 2.1 Transfer Function

The transfer function of the CMOS inverter has 5 distinct regions of operation

1. NMOS off, PMOS linear. This region is defined to be for 0 input voltage up to the point where the NMOS device begins to conduct (Equation 3)

$$V_{IN} \leq V_{TN} \quad (14)$$

2. NMOS saturated, PMOS linear. This region is from when the NMOS device begins to conduct, until the PMOS device changes from being linear to saturated (Equation 4)

$$V_{SD} \leq V_{SG} + V_{TP}. \quad (15)$$

The end of this region can be found by substituting Equations 11 and 12 into Equation 15 to give

$$V_{TN} \leq V_{IN} \leq V_{OUT} + V_{TP} \quad (16)$$

3. NMOS saturated, PMOS saturated. This region comes directly from the regions specified in Equations 5 and 10

$$V_{OUT} + V_{TP} \leq V_{IN} \leq V_{OUT} + V_{TN} \quad (17)$$

4. NMOS linear, PMOS saturated. A similar argument to that of the previous region gives

$$V_{OUT} + V_{TN} \leq V_{IN} \leq V_{DD} + V_{TP} \quad (18)$$

5. NMOS linear, PMOS off.

$$V_{IN} \geq V_{DD} + V_{TP} \quad (19)$$

## 2.2 Gate Switching Threshold

The value of  $V_M$  is defined at that where  $V_{IN} = V_{OUT}$ . When this occurs, both transistors are saturated. Thus

$$I_{DSN} = -I_{DSP} \quad (20)$$

$$\frac{K_N}{2}(V_{GSN} - V_{TN})^2 = \frac{K_P}{2}(V_{GSP} + V_{TP})^2 \quad (21)$$

$$\frac{K_N}{2}(V_M - V_{TN})^2 = \frac{K_P}{2}(V_{DD} - V_M + V_{TP})^2 \quad (22)$$

$$V_M - V_{TN} = \sqrt{\left(\frac{K_P}{K_N}\right)}(V_{DD} - V_M + V_{TP}) \quad (23)$$

$$V_M = \frac{r(V_{DD} + V_{TP}) + V_{TN}}{1 + r} \quad (24)$$

where  $r = \sqrt{\left(\frac{K_P}{K_N}\right)}$ . Note that for a symmetrical transfer function,  $V_{TP} = -V_{TN}$  and  $K_P = K_N$ .

### 2.3 Noise Margin

The CMOS inverter has rail-to-rail outputs which means that  $V_{OL} = 0V$  and  $V_{OH} = 5V$ . The  $V_{IL}$  and  $V_{IH}$  points are defined by the points on the DC transfer function where  $\frac{\partial V_{OUT}}{\partial V_{IN}} = -1$ . The low and high level noise margins are simply

$$NM_L = V_{IL} - V_{OL} \quad (25)$$

$$NM_H = V_{OH} - V_{IH} \quad (26)$$

In the case of  $V_{IL}$ , the PMOS device is in the linear region of operation and the NMOS device is saturated. Also, Equation 13 must hold so

$$\frac{K_N}{2}(V_{GS} - V_{TN})^2 = K_P((V_{SG} + V_{TP})V_{SD} - \frac{V_{SD}^2}{2}). \quad (27)$$

Noting that  $V_{GSN} = V_{IN}$ , using Equations 11 and 12 gives

$$\frac{K_N}{2}(V_{IN} - V_{TN})^2 = K_P((V_{DD} - V_{IN} + V_{TP})(V_{DD} - V_{OUT}) \quad (28)$$

$$- \frac{(V_{DD} - V_{OUT})^2}{2}). \quad (29)$$

Differentiating both sides with respect to  $V_{IN}$  gives

$$K_N(V_{IN} - V_{TN}) = K_P((V_{DD} - V_{IN} + V_{TP})(-\frac{\partial V_{OUT}}{\partial V_{IN}}) \quad (30)$$

$$-(V_{DD} - V_{OUT}) - (V_{DD} - V_{OUT})(-\frac{\partial V_{OUT}}{\partial V_{IN}})) \quad (31)$$

At  $V_{IN} = V_{IL}$ ,  $\frac{\partial V_{OUT}}{\partial V_{IN}} = -1$  so

$$K_N(V_{IN} - V_{TN}) = K_P(2V_{OUT} - V_{IN} - V_{DD} + V_{TP}) \quad (32)$$

so at  $V_{IN} = V_{IL}$

$$V_{IN} |_{V_{IL}} = \frac{2V_{OUT} - V_{DD} + V_{TP} + \frac{K_N}{K_P}V_{TN}}{1 + \frac{K_N}{K_P}} \quad (33)$$

This is an equation with 2 unknowns, namely  $V_{IN}$  and  $V_{OUT}$ . We must simultaneously solve the linear equation Equation 33 with the quadratic equation Equation 28 to obtain  $V_{IN}$  and  $V_{OUT}$  at  $V_{IL}$ . This can be done numerically by forming an optimization problem (see below for an example).

For the case of  $V_{IH}$  the NMOS device is in the linear region of operation and the PMOS device is saturated. Thus

$$K_N((V_{GS} - V_{TN})V_{DS} - \frac{V_{DS}^2}{2}) = \frac{K_P}{2}(V_{SG} + V_{TP})^2 \quad (34)$$

Noting that  $V_{GSN} = V_{IN}$ , using Equations 11 and 12 and gives

$$K_N((V_{IN} - V_{TN})V_{OUT} - \frac{V_{OUT}^2}{2}) = \frac{K_P}{2}((V_{DD} - V_{IN}) + V_{TP})^2 \quad (35)$$

differentiating both sides with respect to  $V_{IN}$  gives

$$K_N((V_{IN} - V_{TN})\frac{\partial V_{OUT}}{\partial V_{IN}} + V_{OUT} - V_{OUT}\frac{\partial V_{OUT}}{\partial V_{IN}}) = -K_P((V_{DD} - V_{IN}) + V_{TP}) \quad (36)$$

At  $V_{IN} = V_{IH}$ ,  $\frac{\partial V_{OUT}}{\partial V_{IN}} = -1$  so

$$K_N(-(V_{IN} - V_{TN}) + V_{OUT} + V_{OUT}) = -K_P((V_{DD} - V_{IN}) + V_{TP}) \quad (37)$$

so at  $V_{IN} = V_{IH}$

$$V_{IN} |_{V_{IH}} = \frac{2V_{OUT} + V_{TN} + \frac{K_P}{K_N}(V_{DD} + V_{TP})}{1 + \frac{K_P}{K_N}} \quad (38)$$

This is an equation with 2 unknowns, namely  $V_{IN}$  and  $V_{OUT}$ . We can simultaneously solve the linear equation Equation 38 with the quadratic equation Equation 35 using numerical methods.

An optimization problem can be formed to find  $V_{IH}$ . Firstly, the function

$$f1(V_{IN}, V_{OUT}) = |V_{IN} - \frac{2V_{OUT} + V_{TN} + \frac{K_P}{K_N}(V_{DD} + V_{TP})}{1 + \frac{K_P}{K_N}}| \quad (39)$$

is formed. A zero of this function means that Equation 38 is satisfied. Similarly,

$$f2(V_{IN}, V_{OUT}) = |K_N((V_{IN} - V_{TN})V_{OUT} - \frac{V_{OUT}^2}{2}) - \frac{K_P}{2}((V_{DD} - V_{IN}) - V_{TP})^2| \quad (40)$$

is formed from Equation 35. If a zero of the function

$$f(V_{IN}, V_{OUT}) = f1(V_{IN}, V_{OUT}) + f2(V_{IN}, V_{OUT}) \quad (41)$$

can be found, this will simultaneously satisfy both equations.

The following MATLAB program performs this computation.

```
function err = vih(IN);
% function err = vih(IN);
% error function for computing VIH, if you can minimise this
% function with sensible values for the input [VIH VOUT]
% then you have the VIH, VOUT values which satisfy both
% equations simultaneously
% CALL WITH fmins('vih', [4 1], [1 1e-8 1e-8])

VIH = IN(1); VOUT = IN(2);
VTN = 0.70; VTP = -0.91;
KN = 50e-6; KP = 20e-6;
x = KP/KN;
VDD = 5;

err1 = abs(VIH - ((2*VOUT + VTN) + x*(VDD - abs(VTP))))
    / (1 + x);
err2 = abs(KN*((VIH - VTN)*VOUT - VOUT*VOUT/2)
    - 0.5*KP*((VDD - VIH - abs(VTP))^2));
err = err1 + err2;
```

## 2.4 Propagation Delay

The propagation delay for a high to low output transition of the CMOS inverter,  $t_{PHL}$ , depends only on the properties of the NMOS transistor. It can be described by the differential equation

$$-C_L \frac{dV_{OUT}}{dt} = I_{DSN} \quad (42)$$

A crude solution can be made by using a linear approximation. The current values at the start and end of the transition are averaged to give

$$I_{DSN}(average) = \frac{1}{2}(I_{DSN}(V_{IN} = V_{OH}, V_{OUT} = V_{OH}) \quad (43)$$

$$+ I_{DSN}(V_{IN} = V_{OH}, V_{OUT} = V_{50\%})). \quad (44)$$

A better approximation can be made by integrating Equation 42. During the transition, the transistor is saturated for a time from  $t_0$  to  $t_1$ . Thus

$$t_1 - t_0 = -C_L \int_{V_{OH}}^{V_{OH} - V_{TN}} \frac{1}{\frac{K_N}{2}(V_{OH} - V_{TN})^2} dV_{OUT} \quad (45)$$

$$= \frac{2C_L V_{TN}}{K_N (V_{OH} - V_{TN})^2} \quad (46)$$

From  $t_1$  to  $t_2$ , the transistor is in the linear region of operation. Thus remembering that

$$\int \frac{dx}{ax + bx^2} = \frac{1}{a} \ln\left(\frac{x}{a + bx}\right) \quad (47)$$

we get

$$t_2 - t_1 = -C_L \int_{V_{OH} - V_{TN}}^{V_{50\%}} \frac{1}{K_N((V_{OH} - V_{TN})V_{OUT} - \frac{V_{OUT}^2}{2})} dV_{OUT} \quad (48)$$

$$= -\frac{C_L}{K_N} \frac{1}{(V_{OH} - V_{TN})} \ln \frac{V_{OUT}}{(V_{OH} - V_{TN}) - V_{OUT}/2} \Big|_{V_{OH} - V_{TN}}^{V_{50\%}} \quad (49)$$

$$= -\frac{C_L}{K_N} \frac{1}{(V_{OH} - V_{TN})} (\ln \frac{V_{50\%}}{(V_{OH} - V_{TN}) - V_{50\%}/2} - \ln(2)) \quad (50)$$

$$= \frac{C_L}{K_N} \frac{1}{(V_{OH} - V_{TN})} \ln\left(\frac{2(V_{OH} - V_{TN}) - V_{50\%}}{V_{50\%}}\right) \quad (51)$$

The high to low propagation delay to a step input can be derived by summing Equations 46 and 51 to give

$$t_{stepPHL} = \frac{2C_L V_{TN}}{K_N (V_{OH} - V_{TN})^2} + \frac{C_L}{K_N (V_{OH} - V_{TN})} \ln\left(\frac{2(V_{OH} - V_{TN}) - V_{50\%}}{V_{50\%}}\right) \quad (52)$$

An analogous derivation can be made for the PMOS device to get the low to high propagation delay to a step input

$$t_{stepPLH} = \frac{2C_L |V_{TP}|}{K_P (V_{OH} - V_{OL} + V_{TP})^2} \quad (53)$$

$$+ \frac{C_L}{K_P (V_{OH} - V_{OL} + V_{TP})} \ln\left(\frac{2(V_{OH} - V_{OL} + V_{TP}) - V_{50\%}}{V_{50\%}}\right) \quad (54)$$

The rise and fall times ( $t_r$  and  $t_f$ ) are defined by the time it takes to go from 10% to 90% of the final value. They can be derived from the same linear approximation or integrals as the propagation delays above, with the limits changed.

The values  $tstep_{PHL}$  and  $tstep_{PLH}$  are not particularly useful in practice since they assume a step input. In reality, the devices are driven by other devices with finite rise and fall time. A useful approximation to the real propagation delays  $t_{PLH}$  and  $t_{PHL}$  which takes this into account is

$$t_{PLH} = \sqrt{(tstep_{PLH}^2 + (\frac{t_f}{2})^2)} \quad (55)$$

$$t_{PHL} = \sqrt{(tstep_{PHL}^2 + (\frac{t_r}{2})^2)} \quad (56)$$