

CEG3470 – Digital Circuits (Fall 2009)

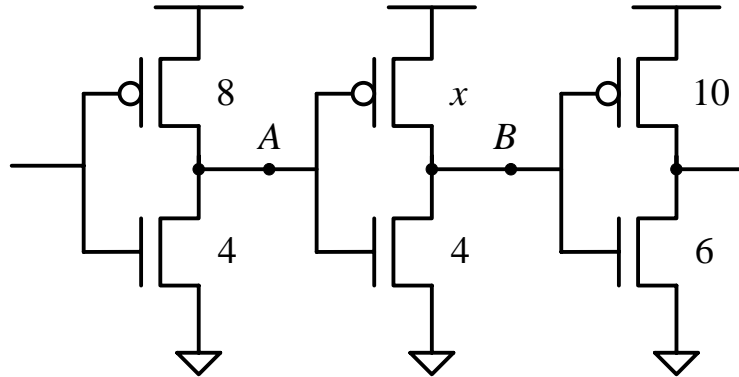
Assigned: Oct 09, 2009

Total Mark: 50

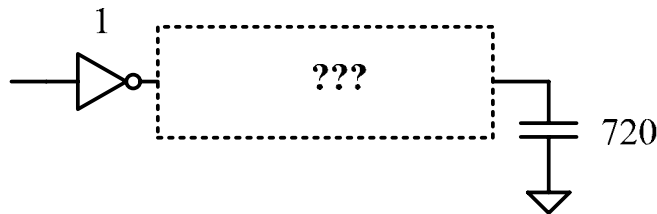
Due: Oct 22, 2009

Homework 1: Inverter Chain Optimization, Logical Effort

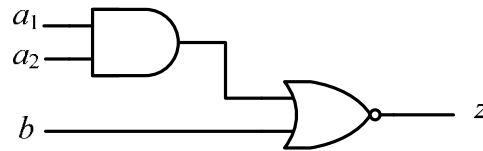
- [5 marks] What is the value of x that can **minimize** the sum of the signal rising time and falling time at point B driven from A?
Given $R_p = 2R_n$. All sizes shown are respective to minimum size inverter.



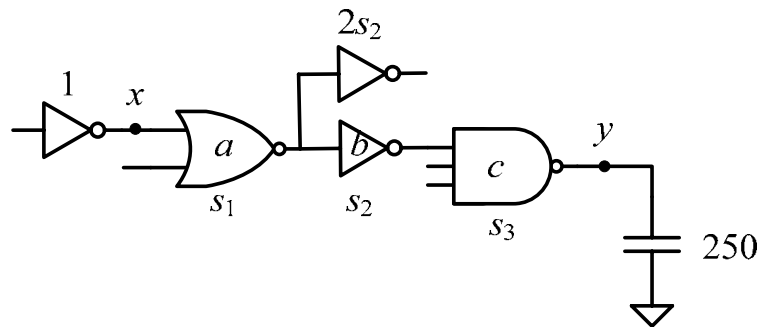
- [15 marks] Design a buffer (inverter chain) that minimize the delay for a min.-size inverter to drive a capacitive load $C_L = 720C_{g,inv}$, where $C_{g,inv}$ is the input capacitance of a min.-size inverter.
Choose and suggest the sizes of the inverters in integers (which is true in practice).
Calculate the corresponding delay with your chosen sizes.



3. [15 marks] The following figure shows an **AOI21** gate which is commonly available in CMOS standard cell library. The gate implements the function $z = \overline{a_1 \cdot a_2 + b}$



- (a) Draw the CMOS schematic of the gate. Show the sizings of all transistors such that its speed performance is the same as a min.-size inverter.
- (b) Write the delay formula for the gate using logical effort.
- (c) Sketch a CMOS layout of the gate using stick diagram. Use **ONLY** poly(red), nidff(green), pdiff(brown), m1(blue), m2(purple) and contacts.
4. [15 marks] An min.-size inverter is driving a load of $250C_{g,inv}$ through gates a , b and c . Using logical effort, find the optimal sizings for s_1 , s_2 and s_3 that minimizes the delay from x to y . Calculate the optimal delay.



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