

## CEG3470 – Digital Circuits (Fall 2009)

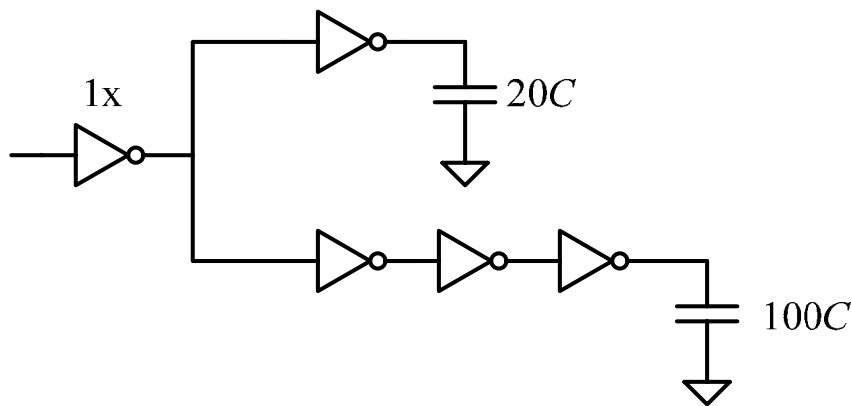
Assigned: Oct 06, 2009

### Class Drill: Inverter Chain Optimization and Logical Effort

The exercises are adapted from UCB EE141 Homework 2 and 3 (Spring 2009).

#### Question 1

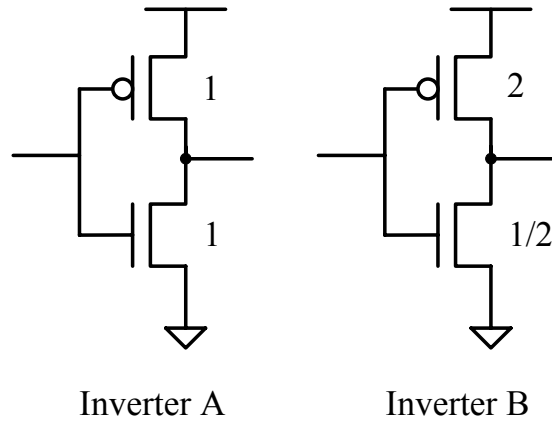
Following schematic exemplifies a (heavily) simplified clock distribution network. The first inverter is of minimum size (1x). Input capacitance of a minimum-size inverter is  $C$ . Assume  $\gamma = 1$ .



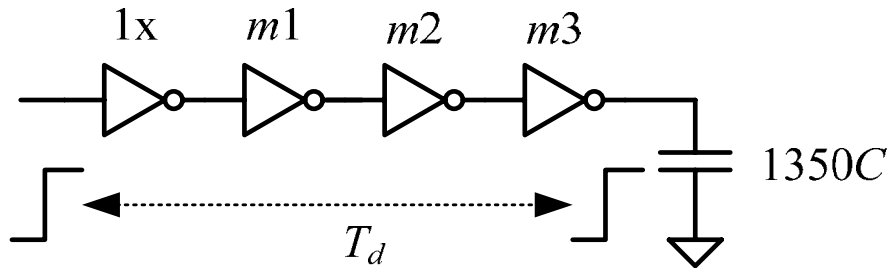
- Suppose that the top path with  $20C$  loading is the critical path, which you care the most about its propagation delay. Size the rest of the inverters in the figure to minimize the delay. Feel free to say “don’t care” if there are inverters that you don’t care about their sizing.
- Repeat part (a), assuming that the bottom path with  $100C$  is the critical path instead.
- Finally assume that both paths are equally critical. Size the inverters so that the average of the two delays is minimized.

Question 2

We sometimes design the inverter to favor one transition. Fig. 1 shows two examples with unequal rising and falling delays.



- (a) Calculate the logical effort of the skewed inverters shown above for both **rising** and **falling** output transitions. Which inverter does favor rising output transition? Why?
- (b) Suppose the skewed inverters shown in the figure are included in your digital cell library. Choose and design the inverters  $m1$ ,  $m2$ ,  $m3$  to minimize the delay  $T_d$  for the low-to-high input transition, as shown below. Also calculate the delay  $T_d$  and the corresponding high-to-low input transition.



- End -