

Triple patterning in 10nm node metal lithography

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Next-generation lithographic methods will have major implications for 10nm logic in terms of physical design, design rules, and mask synthesis/electronic design automation algorithms.

The local metallization layers of logic products are historically the densest layouts to lithographically pattern and are key drivers of product density (and therefore cost). Due to delays in extreme-UV (EUV) lithography and difficulties in applying other resolution-enhancement technologies (RETs)—such as double-patterning methods—triple-patterning technology (TPT) is a strong option for handling the local metal layers of the upcoming 10nm logic technology node (~44–48nm minimum feature pitch). Several TPT methods, including ones developed by us, are being considered in different product areas of semiconductor manufacturing.^{1,2} For advanced logic metal layers, the main TPT option assumes a process flow known as litho-etch-litho-etch-litho-etch (LELELE). In this flow, the final substrate pattern is the logical OR of three successive lithography+etch sequences, each sequence using a single traditional lithography+etch sequences, each sequence using a single traditional lithography exposure and a single etch step (see Figure 1).

The use of LELELE TPT in a product design and production flow involves the following steps: design of TPT-compliant layout; design verification; decomposition of the layout into the three TPT single-exposure wafer targets (via TPT decomposition software); RET/optical proximity correction (OPC) steps for each single-exposure wafer target; OPC verification; mask data preparation; mask manufacture; and wafer processing in the fabrication facility (fab). There are many difficulties in achieving a high-yielding, cost-effective TPT process. Here, we first look at problems in mask manufacture and wafer production flow, especially cost, turn-around time, and the logistical challenges of tripling the number of mask and fab process steps per layer. However, the complexity and process control requirements of a TPT mask and wafer flow also increase substantially. Moreover, potential negative interactions can cause device failure between feature edge placements from the different litho-etch

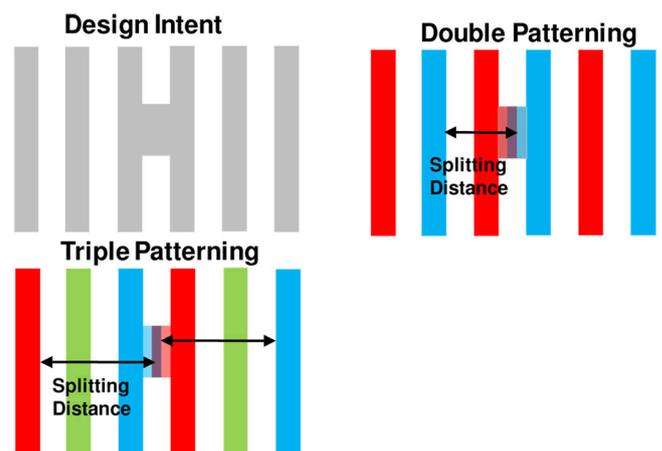


Figure 1. Examples of metal routing configuration in design and with double (DPT) and triple patterning technology (TPT), showing the potentially large benefit for pattern density of triple patterning for 1D features. The different colors of the polygon in the decomposed layouts represent the different mask target layouts (two masks for DPT, three masks for TPT).

steps.³ Consequently, individual feature critical dimension (CD) and overall control tolerances in a TPT process must be significantly tighter than in a single-exposure process for the same device layer.

Design and mask synthesis (i.e., decomposition, RET, OPC, and OPC verification) pose different but related difficulties. Designers must be able to confidently create and verify TPT-compliant layouts. This requires accurate and sufficiently flexible design rules. Figure 2 shows examples of basic TPT design rules for the metal1 layer of standard cells. The design flow must also be able to quickly and accurately verify the physical and electrical integrity of the full-chip final design target. Mask synthesis cost and turn-around time are definitely affected by the tripling of the number of processing steps. However, a bigger risk would be if the increased accuracy requirements could not be met. Fortunately, the RET, OPC, and OPC verification

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methods developed for DPT can be extended to successfully handle TPT requirements in these areas.

An even more fundamental TPT mask synthesis challenge exists in the layout decomposition step. Production-worthy TPT decomposition methods are not yet fully defined and validated. Currently, the two most plausible approaches are extension of existing DPT decomposition methods (see Figure 3), and development of full TPT decomposition algorithms. The advantage of the first approach is that DPT methods are well known, trusted, available, and fast enough to run on full-chip layouts. A main drawback is that it is less likely to result in a decomposition solution for layouts that are TPT compliant. This can lead to a TPT-compliant design being decomposed in an unmanufacturable manner. Another drawback of extending existing DPT methods is difficulty in achieving similar feature density for all three masks. Mask density imbalance can lead to degraded overlay and CD control.

We have proposed several TPT decomposition algorithms.² The quality of results can vary strongly, as better algorithms can enlarge the set of layouts that are TPT-compliant, leading to solutions that have a smaller layout area and are more manufacturable (see Figure 4).⁴ The main drawback of full TPT algorithms is that their turn-around time/memory performance is not yet sufficient for full-chip decomposition (see Figure 5).⁵ With these performance limitations, the industry must do TPT

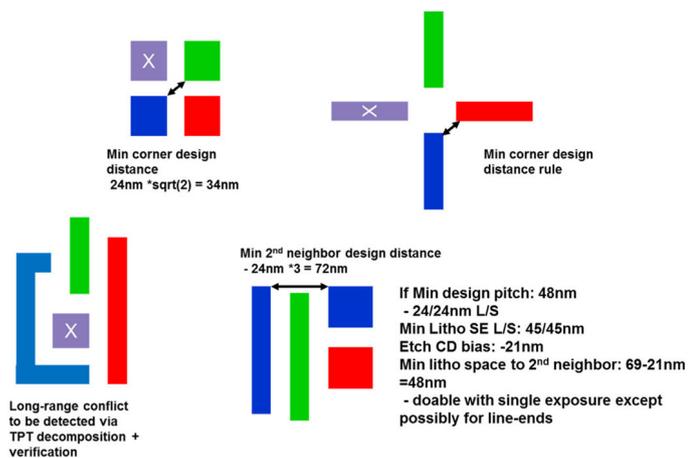


Figure 2. Examples of design rules to detect TPT non-compliant layout for a fictional 48nm minimum pitch process. X indicates a TPT conflict. The long-range TPT conflict at the lower left cannot be found by conventional design rule constraint methods. It requires full TPT decomposition to be run before conflicts can be found. L/S: Line/space. SE: Single exposure. CD: Critical dimension.

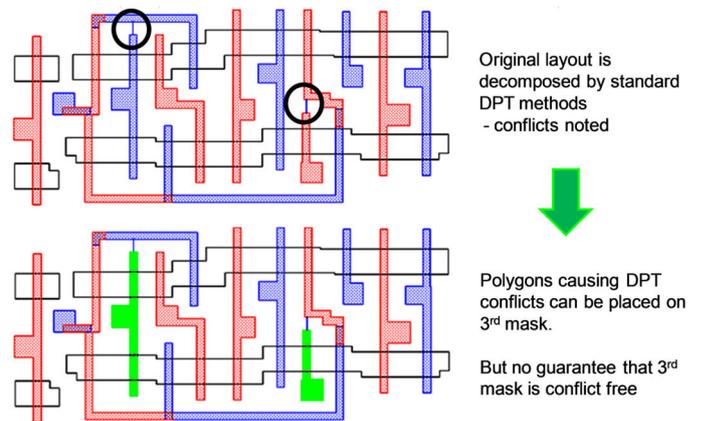


Figure 3. Example showing how DPT methods can be reused to create TPT decomposition. First, a traditional two-color DPT decomposition is run. Next, DPT conflicts are identified. Then, one polygon at each conflict area is transferred to the third mask (color). Finally, each color is checked separately for conflicts (i.e., spacing violations).

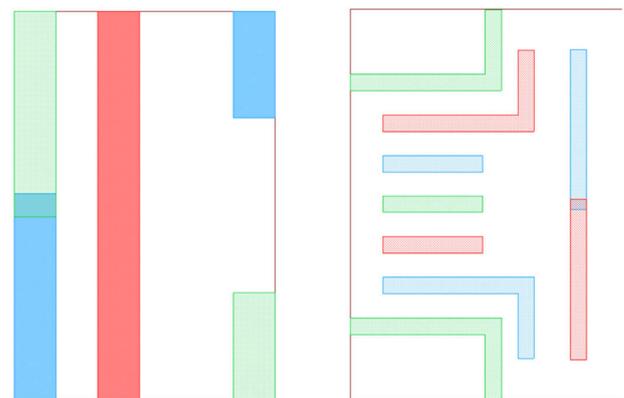
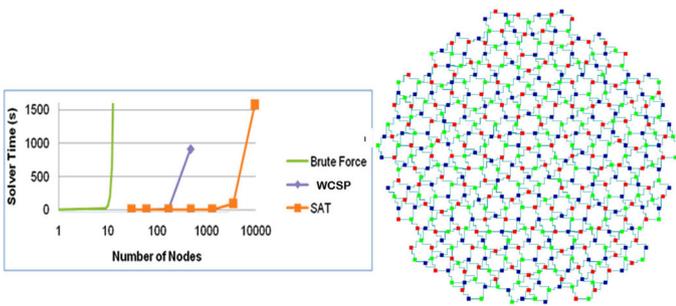


Figure 4. Examples of complex layouts that require a sophisticated TPT algorithm to find a compliant and manufacturable decomposition solution. The need to resolve long-range TPT conflict interactions and determine optimal stitching locations increases the solution space to search and limits the usefulness of simpler TPT solvers.

decomposition individually on smaller cells and layout blocks, then use correct-by-construction design rule and design practice approaches to ensure the entire chip becomes TPT compliant. Fortunately, TPT full-chip compliance can be easily and quickly verified using extensions of existing DPT software (e.g., design rule constraints or OPC verification).

In summary, TPT patterning is a serious option for local metal layers in next-node logic processes. Several design and process



Penrose Rhombic Tiling showing Multiple odd cycle loops.
Requires only 3 colors for compliance.

Figure 5. Example of decomposition algorithm turn-around time (TAT) vs. the number of nodes to color for a known TPT-compliant test pattern.⁵ Full TPT decomposition TAT shows a rapid increase with the number of linked nodes to color in a layout. Smart techniques—such as those we have described elsewhere⁴—can greatly reduce TAT. But full-chip TPT decomposition ability is far from certain. WCSP: Weighted constraint satisfaction problem. SAT: Satisfiability.

techniques developed for DPT can be reused in TPT. However, significant challenges remain. The biggest process challenges are cost and control. The biggest design and mask synthesis challenges are the development and coordinated deployment of TPT decomposition algorithms. Our current work focuses on improving TPT algorithm applicability to larger layout sizes for 10nm node design rule and process integration development.

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