**Split Manufacturing**

The notion of integrated circuit split manufacturing which delegates the front-end-of-line (FEOL) and back-end-of-line (BEOL) parts to different foundries [McCants 2011], is to prevent overproduction, piracy of the intellectual property (IP) [Shamsi et al. 2019], or targeted insertion of hardware Trojans [Li et al. 2018] by adversaries in the FEOL facility.

**Non-proprietary Criteria**

For a VPP (n, q), if q is on the opposite side of one of the wire segments directly connected to p, then say the virtual pin p prefer virtual pin r

Objective correct connection rate:

\[ CCR = \frac{\sum_{i=1}^{n} x_{ii}}{\sum_{i=1}^{n} y_{ii} + \sum_{i=1}^{n} y_{ij}} \]  

where \( x_{ii} \) is the number of sinks in every fragment, \( y_{ii} \) \( y_{ij} \) are the numbers of sinks in every fragment, \( q = 1 \) when a positive virtual pin pair (VPP) is selected for the q-th sink fragment, \( q = 0 \) when a negative VPP is selected for the q-th sink fragment.

**Feature Extraction**

- **Vector-based Features**
  - Distances for VPPs along the preferred and the non-preferred routing direction.
  - Maximum capacitance of the driver and pin capacitance of the sinks.
  - Number of sinks connected within the sink fragment.
  - Wirelength and via contribution in each FEOL metal layer.
  - Driver delay based on the underlying timing paths.

- **Image-based Features**
  - We represent the routing layout of the local regions containing the virtual pin as grayscale layout images. We consider three different scales with the same image shape but different precisions.

Each image is 99 pixels wide and high, representing 99 × 99 consecutive regions. Since wires closer to the BEOL carry more information about the connection, those in higher metal layers are encoded in more significant bits.

**Sample Selection**

We select n candidate VPPs for each sink in training and testing based on three criteria:

1. **Direction Criterion**
   - For a VPP (n, q), if q is on the opposite side of one of the wire segments directly connected to p, then say the virtual pin p prefer virtual pin r.
2. **Non-proprietary Criterion**
   - A VPP is not considered as a candidate in case both source and sink pins do not prefer each other.
3. **Distance Criterion**
   - If the number of VPPs remaining is greater than n, the VPPs with shorter distance in the non-preferred routing direction of the split layer are considered as candidates.

**Model Architecture**

- **Input:** A batch of features corresponding to a sink fragment including the image-based features of the sink fragment itself.
- **Output:** scores for every VPP in the batch.

**Experimental Results**

Comparison between Ours and Wang (TVLSI'18)

<table>
<thead>
<tr>
<th>Model</th>
<th>M1 CCR (%)</th>
<th>M2 CCR (%)</th>
<th>M3 Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ours</td>
<td>0.21</td>
<td>0.12</td>
<td>0.10</td>
</tr>
<tr>
<td>Wang</td>
<td>0.00</td>
<td>0.00</td>
<td>0.00</td>
</tr>
</tbody>
</table>

**Conclusion**

- Demonstrate vector-based and image-based features.
- Process heterogeneous features simultaneously in a neural network.
- Propose a softmax regression loss that directly reflects on the accuracy for the virtual pin pair matching problem of split manufacturing.

**References**