Timing Aware Dummy Fill Insertion

- **Dummy fill insertion**
  - Reduce dielectric thickness variation;
  - Provide nearly uniform pattern density;
  - Highly related to the quality of chemical-mechanical polishing (CMP) process.

Timing-aware Dummy Fill Insertion

- Inserted metal fill as metal sidewall:
  - Improves density, increases planarity;
  - Cons: couples with signal tracks
- Severely affect the original layout timing closure.
- Need to reduce the coupling impact during the metal fill insertion.

**Capacitance Evaluation**

- **Area Capacitance**: Two conductor layers on different metal layers, and their projections overlap $\Rightarrow C^A = P_1(x) \times A$.
- **Lateral Capacitance**: Two conductor layers on the same layer, and have horizontal overlap $\Rightarrow C^L = P_1(d) \times l$.

**Fringe Capacitance**: Two conductor pieces on different layers, and have parallel edge overlap $\Rightarrow C^F = \frac{P_2(\Delta x) \times A_1}{\Delta x} = \frac{P_2(y) \times l}{y}$.

**Fringe criteria** $\Rightarrow C^F = \frac{P_2(\Delta x) \times A_1}{\Delta x} = \frac{P_2(y) \times l}{y} > \gamma d$.

Given a design layout, insert metal fills to minimize:

$$\min \sum \gamma i A_i$$

s.t. Density constraints

$$\gamma d < \gamma d$$

**Overview of FIT Flow**

- **Efficient**: Strong runtime performance on ICCAD 2018 benchmarks.
- **Optimal**: Outperforms the contest winner by all metrics.
- **Extensible**: Separate modules, easy to further integrate other optimization flow.

**Fillable Region Generation**

- Extract fillable polygons of the entire layer.
- Polygon decomposition: polygons with thousands of vertices and maybe holes inside are difficult to handle $\Rightarrow$ decompose them into rectangles, assign rectangles into different windows ($\Rightarrow$ 22813)
- The aspect ratio of rectangle fits the layer preferred direction. Use sweep line to $\Rightarrow$ convert rectangles locally.
- Comparing to [Liu+, TODAES’16], significantly expands the solution spaces for later procedures.

**Target Density Planning (TDP)**

- The window $\Rightarrow$ commit those fills that close to window border to global checker.

**Global Fill Synthesis (GFS)**

- Offload any area overlap between fill and the given critical wires.
- Order-Sensitive process, obtain a better insertion order.
- Order: $\Rightarrow$ sort the windows order by the density gap $\Delta D = D - D_{\text{norm}}$.
- Fringe checker responsible for insertion and legalization of a specific window, discard when finished.
- Global checker keeps wire locations for the entire layout ($\Rightarrow$ one partitioned region of the layer), success insertion of a window only commits those fills that close to window border to global checker.

**Detailed Post Refinement (DPR):**

- Relocate those fills (obtained from GFS) with high impact on timing:

$$\min \sum \gamma i A_i$$

s.t. Density and max fillable area constraints

$$\gamma d < \gamma d$$

**Design rules**

- Minimum spacing, maximum fill width, and maximum fill length.

Additionally, the total parasitic capacitance of all signal nets is also considered, since it will affect performance like power consumption, timing.

* Equivalently to the ground, can be obtained by network acyclic method.

**Global Fill Synthesis and Legalization**

- An efficient heuristic window-based flow for high quality initial solution.
- Guided by the target density scheduling result.
- Only performing the GFS flow can already beat the contest winner results.

**Insertion criteria**

- Increase the spacing and reduce the parallel overlap lengths between any two metal conductors.
- Forbidden any area overlap between fill and the given critical wire.
- Order- Sensitive process, obtain a better insertion order.
- Order: $\Rightarrow$ sort the windows order by the density gap $\Delta D = D - D_{\text{norm}}$.
- Sort the fills rectangles by weighted score of their shape, area, distance, and parallel overlap to/with surrounding critical wires.

$$\Delta D = D - D_{\text{norm}} = \alpha + \beta \gamma + \sqrt{\gamma^2 + \frac{1}{4}}$$

**Legalization**

- A design rules checker (RTWme) is maintained to perform legalization and record density.
- Noise implementation: insert all wires and fills into checker $\Rightarrow$ Time consuming.
- Pruning: Global checker = local checkers.
- Local checker responsible for insertion and legalization of a specific window, discard when finished.
- Global checker keeps wire locations for the entire layout (or one partitioned region of the layer), success insertion of a window only commits those fills that close to window border to global checker.

**Detailed Post Refinement**

- Timing-aware Fill Relocation:

$$\min \sum \gamma i A_i$$

s.t. Density and max fillable area constraints

$$\gamma d < \gamma d$$

**Design rules**

- Minimum spacing, maximum fill width, and maximum fill length.

- Alternately optimize for X-dimension and Y-dimension:

$$\min \frac{D - \sum \gamma i A_i}{D}$$

s.t. Density constraints

$$\gamma d < \gamma d$$

**Shifting refinement** is regardless of original fillable region limitations.

**Experimental Results**

- On ICCAD 2018 Contest Benchmarks

<table>
<thead>
<tr>
<th>Case</th>
<th>Critical nets</th>
<th>1st Place Team</th>
<th>FIT</th>
<th>Improvement</th>
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<td>1</td>
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<td>7632.02</td>
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</table>

**Windows average density upper bound**

<table>
<thead>
<tr>
<th>Case</th>
<th>Density (Case 1)</th>
<th>Density (Case 2)</th>
<th>Density (Case 3)</th>
<th>Density (Case 4)</th>
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**Target Density Planning**

Objective: distribute the target density for each window (under density constraint).

- Divide original window $(w \times w)$ into 4 sub-windows with size of $\frac{w}{2} \times \frac{w}{2}$.
- Reduce the critical nets capacitance and total wire capacitance.

$$\min \frac{1}{w} \sum_{i=1}^{m} (\sum_{j=1}^{n} C_{ij} - \min \{\sum_{j=1}^{n} C_{ij}^{\text{max}} - D_{ij}\})$$

s.t. Density constraints

$$\frac{w}{2} \times \frac{w}{2} \Rightarrow C^F = \frac{P_2(\Delta x) \times A_1}{\Delta x} > \gamma d$$

- Weight $\Omega_i$ measures the criticality of window $W_i$ (the ratio of critical wires enclosed in).

$$\Omega_i = \left\{ \begin{array}{ll} 1 & \text{if} \quad \Omega_i > 0, \quad \Omega_i^0 = 0, \\ \omega^0 & \text{else.} \end{array} \right.$$