DSAR: DSA aware Routing with Simultaneous DSA Guiding Pattern and Double Patterning Assignment

Jiaojiao Ou\textsuperscript{1}, Bei Yu\textsuperscript{2}, Xiaoqing Xu\textsuperscript{1}, Joydeep Mitra\textsuperscript{3}, Yibo Lin\textsuperscript{1}, David Z. Pan\textsuperscript{1}

\textsuperscript{1}\textsc{ECE} Department, University of Texas at Austin
\textsuperscript{2}\textsc{CSE} Department, CUHK
\textsuperscript{3}Mentor Graphics Inc.
Outline

- Introduction
- Problem formulation
- Detailed routing algorithms
- Experimental results
- Conclusion
Introduction: Technology Scaling

[Diagram showing the progression of technology scaling from 2005 to 2025, with labels for Transistors, Patterning, Interconnect, and Complexity. Key technologies include Planar CMOS, FinFET, Cu Doping, EUV, Graphene, and 3D IC.]
Technology Scaling: More Masks

♦ Via density increases

✓ Triple/Quadruple patternings are required
  • Placement error problem
  • Cost increases
✓ More via: 1D design

(a) Original layout
(b) Via layer with quadruple patterning

Via density increases

Triple/Quadruple patternings are required

• Placement error problem
• Cost increases

More via: 1D design

$$MIN_{\text{litho}} = 3 \cdot L_{\text{grid}}$$
Motivation of DSA on Via Layer

- Reduce mask number by grouping vias in the same guiding pattern

Reduce 2 mask with DSA 😊
Consider DSA during Routing 1

- Initial detailed routing without DSA consideration
  - 3 masks are required
Consider DSA during Routing 2

♦ Initial detailed routing without DSA consideration
  ✔ 3 masks are required

♦ Reroute n1 and n3
Consider DSA during Routing 3

- Initial detailed routing without DSA consideration
  - 3 masks are required
- Reroute n1 and n3
  - Reduce 1 more mask 😊
Previous Works

♦ DSA-aware detailed routing for via layer optimization [Du+, SPIE’14]
  ✓ Resolve conflicts and infeasible via patterns during rip-up and reroute with negotiated congestion based scheme
  ✓ Incapable to handle DSA with multiple patternings
  ✓ More wire length may be introduced

♦ Redundant Via insertion consideration [Lin+, ASPDAC’17]
  ✓ Simultaneously consideration of redundant via insertion and guiding template feasibility
  ✓ Increase redundant via insertion rate
  ✓ Multiple patterning for via is not considered, not compatible for 1D design
### Problem Formulation: DSAR

**DSA and double patterning aware detailed routing**

**Input:**
- Netlist with source/target pins
- Feasible DSA patterns
- Design rules

**Output:**
- Minimize wirelength, unroutable nets
- DSA-DP compatible via layer
Design Rules

DSA design rules

\[ L_{\text{grid}} > MIN_{dsa} \quad 2 \cdot L_{\text{grid}} \leq MAX_{dsa} < 3 \cdot L_{\text{grid}} \]

Feasible region: \( MIN_{dsa} \rightarrow MAX_{dsa} \rightarrow MIN_{litho} \)

More complex guiding templates

Forbidden Via distribution

- Metal 2
- Metal 3
- Via
- Cut mask

\[ l < MIN_{area} \]
Pre-route Net Planning - 1

Construct conflict graph

- Vertices: bbox corners
- Edge weight: DSA friendly? 1: 5
Pre-route Net Planning - 1

♦ Construct conflict graph

✓ Vertices: bbox corners
✓ Edge weight: DSA friendly? 1: 5
Construct conflict graph

- Vertices: bbox corners
- Edge weight: DSA friendly? 1: 5
Pre-route Net Planning - 1

♦ Construct conflict graph

✓ Vertices: bbox corners
✓ Edge weight: DSA friendly? 1: 5
Construct conflict graph

- Vertices: bbox corners
- Edge weight: DSA friendly? 1: 5
Construct conflict graph

✓ Vertices: bbox corners
✓ Edge weight: DSA friendly? 1: 5
Construct conflict graph

- Vertices: bbox corners
- Edge weight: DSA friendly? 1: 5
Construct conflict graph

- Vertices: bbox corners
- Edge weight: DSA friendly? 1: 5
Conflict graph constraints
- At most 1 corner of each net
Conflict graph constraints

- At most 1 corner of each net
- Corners cross the pins of other nets
Conflict graph constraints

- At most 1 corner of each net
- Corners cross the pins of other nets

Conflict graph bipartization

- Pre-determine (estimate) the routing paths for nets
Pre-route Net Planning - 3

- Conflict graph constraints
  - At most 1 corner of each net
  - Corners cross the pins of other nets

- Conflict graph bipartization
  - Pre-determine (estimate) the routing paths for nets
  - Minimize deleted vertices from conflict graph
    - DSA unfriendly vertices

\[
\min \sum_{i=1}^{N} (\alpha_i \times c_i)
\]
\[
\alpha_v = \frac{1}{\sum_{e \in V} \text{Cost}_e}
\]

\[
\begin{align*}
\text{s.t.} & \quad s_v + s_u + (c_v + c_u) \geq 1, & \forall \{v, u\} \in E_s, \\
& \quad s_v + s_u - (c_v + c_u) \leq 1, & \forall \{v, u\} \in E_s, \\
& \quad c_v + c_u \geq 1, & \forall \{v, u\} \in E_d, \\
& \quad c_v = 1, & \forall v \in V_f.
\end{align*}
\]
Net ordering for undetermined nets

- Smaller bbox (HPWL)
- Overlaps

Route b first

Route a first

More WL
Routing graph model

- One color assignment forbidden
- Via inserted
- All vias are forbidden
Detailed Routing - 2

Routing box state update

Nearby routing box update

Example

Green via  Red via  Red via is forbidden  Empty via
All via forbidden grid  Green via is forbidden  M2  M3
Routing scheme

- Negotiated congestion based
- A* search

\[ p_i(s, t) = c(i) + \sigma \times \text{dist}_i^t \]
\[ c(i) = \text{cost}_{s-1}^i + c_{i-1}^i + h(i) \]
\[ h(i) = h(i)' + A \times \text{usage}(i) + B \times h_{\text{dsa}}(i) \]
\[ \sigma = \begin{cases} 1, & \text{if } c(i) \leq l_{\text{HPWL}}, \\ 1 + \frac{c(i)}{H \text{PWL}}, & \text{if } c(i) > l_{\text{HPWL}}. \end{cases} \]

Algorithm 1 DSA+DP aware detailed routing

**Input:** Netlists from net planning algorithm.

**Output:** Routed nets with DSA friendly via layer.

1. Route determined nets;
2. Update grids cost;
3. Initial routing iteration;
4. \( Q \leftarrow \) nets in violated grids;
5. \textbf{while} \ !Q.empty() \textbf{do}
6. \( g(i) \leftarrow Q\text{.pop(); } Nets \subseteq g(i); \)
7. \textbf{for} each net \( k \in Nets \textbf{ do} \)
8. \quad Pre-route with cost evaluation;
9. \textbf{end for}
10. Rip-up net \( k \) that has maximum cost improvement;
11. Route net \( k; \)
12. \textbf{for} each grid \( g(j) \) of net \( k \textbf{ do} \)
13. \quad Update grid cost;
14. \quad \textbf{if} \( g(j) \) is violated \textbf{ then} \)
15. \quad \quad \( Q \leftarrow \) nets in this \( g(j); \)
16. \quad \textbf{end if}
17. \textbf{end for}
18. \textbf{if} \( g(i) \) is still violated \textbf{ then} \)
19. \quad \( Q \leftarrow g(i); \)
20. \textbf{end if}
21. \textbf{end while}
Routing scheme

✓ Negotiated congestion based
✓ A* search

\[ p_i(s, t) = c(i) + \sigma \times \text{dist}^i_s \]

\[ c(i) = \text{cost}^{i-1}_s + c^i_{i-1} + h(i) \]

\[ h(i) = h(i)' + A \times \text{usage}(i) + B \times h_{dsa}(i) \]

\[ \sigma = \begin{cases} 
1, & c(i) \leq l_{HPWL}, \\ 
1 + \frac{c(i)}{HPWL}, & c(i) > l_{HPWL}.
\end{cases} \]

---

Algorithm 1 DSA+DP aware detailed routing

**Input:** Netlists from net planning algorithm.

**Output:** Routed nets with DSA friendly via layer.

1: Route determined nets;
2: Update grids cost;
3: Initial routing iteration;
4: \( Q \leftarrow \) nets in violated grids;
5: \textbf{while} \ !\text{Q.empty}() \textbf{do}
6: \( g(i) \leftarrow \text{Q.pop}(); \quad \text{Nets} \subseteq g(i); \)
7: \textbf{for} each net \( k \in \text{Nets} \textbf{do} \)
8: \quad Pre-route with cost evaluation;
9: \textbf{end for}
10: Rip-up net \( k \) that has maximum cost improvement;
11: Route net \( k \);
12: \textbf{for} each grid \( g(j) \) of net \( k \) \textbf{do}
13: \quad Update grid cost;
14: \quad \textbf{if} \( g(j) \) is violated \textbf{then}
15: \quad \quad \text{Q} \leftarrow \text{nets in this} \ g(j);
16: \quad \textbf{end if}
17: \textbf{end for}
18: \textbf{if} \( g(i) \) is still violated \textbf{then}
19: \quad \text{Q} \leftarrow g(i);
20: \textbf{end if}
21: \textbf{end while}
Post Routing Optimization

- Assign DSA guiding patterns
  - Minimize DSA groups and conflicts
  - Edge bipartization
Post Routing Optimization

- Assign DSA guiding patterns
  - Minimize DSA groups and conflicts
  - Edge bipartization

\[
\begin{align*}
\text{min} & \quad \sum e_{v_iv_j} + M \cdot \sum e_{v_kv_h} \\
\text{s.t.} & \quad t_{v_i} + t_{v_j} + e_{v_iv_j} \geq 1, \quad \forall \{e_{v_iv_j}\} \in E, \\
& \quad t_{v_i} + t_{v_j} - e_{v_iv_j} \leq 1, \quad \forall \{e_{v_iv_j}\} \in E, \\
& \quad e_{v_iv_j} + e_{v_iv_k} \leq 1, \quad \forall (i, j, k) \text{ infeasible}, \\
& \quad e_{v_iv_j} + e_{v_jv_k} + e_{v_kv_h} \leq 2, \quad \forall (i, j, k), (j, k, h) \text{ groupable}, \\
& \quad e_{v_iv_j}, t_{v_i} \in \{0, 1\}. \quad (7f)
\end{align*}
\]
Experimental Setup

- Implemented in C++
- 3.4GHz Linux server, 32GB RAM
- ILP solver: GUROBI 6.5
- OpenSparc T1 design:
  - M2, M3 for routing
  - [Du+, SPIE’14], 1D router

<table>
<thead>
<tr>
<th>bench</th>
<th>#net</th>
<th>#pin</th>
<th>Grid size</th>
</tr>
</thead>
<tbody>
<tr>
<td>ecc</td>
<td>1671</td>
<td>3342</td>
<td>436×446</td>
</tr>
<tr>
<td>efc</td>
<td>2219</td>
<td>4438</td>
<td>406×421</td>
</tr>
<tr>
<td>ctl</td>
<td>2706</td>
<td>5412</td>
<td>496×503</td>
</tr>
<tr>
<td>alu</td>
<td>3108</td>
<td>6216</td>
<td>406×408</td>
</tr>
<tr>
<td>div</td>
<td>5813</td>
<td>11626</td>
<td>636×646</td>
</tr>
<tr>
<td>top</td>
<td>22201</td>
<td>44402</td>
<td>1176×1179</td>
</tr>
</tbody>
</table>
Routing Result Comparison

(a) Number of Vias

(b) Wirelength

(c) DSA conflicts

(d) CPU(s)
Routing Result Comparison

(a) Number of Vias
(b) Wirelength
(c) DSA conflicts
(d) CPU(s)
Routing Result Comparison

(a) Number of Vias

(b) Wirelength

(c) DSA conflicts

(d) CPU(s)

(a) Number of Vias

(b) Wirelength

(c) DSA conflicts

(d) CPU(s)
Routing Result Comparison

(a) Number of Vias

(b) Wirelength

(c) DSA conflicts

(d) CPU(s)
Comparison between W/ and WO Net Planning

(a) Number of Vias

(b) Wirelength

With v.s. without net planning

▷ 19% less via number
▷ 8% less wirelength
▷ 7% more runtime
Conclusion

♦ DSA and double patterning for via layer in detailed routing

✔ Pre-route net planning
✔ Routing model with DSA-DP consideration
✔ Post-routing optimization to improve DSA guiding pattern assignment and decomposition

♦ Future work

✔ Adaptive to more routing layers
✔ General to more DSA and multiple patterning considerations
Q&A

THANK YOU