Standard Cell Layout Regularity and Pin Access Optimization Considering Middle-of-Line

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Outline

Introduction and Problem Formulation

Algorithms

Experimental Results

Conclusion and Future Work
Moore’s Law to Extreme Scaling
Lithography Status & Challenges

[Diagram showing Lithography status with annotations: Rounding, Disappearance, Pinch, Pullback.]

[Courtesy Intel]
Lithography Status & Challenges

[Image of lithography with terms: Rounding, Disappearance, Pinch, Pullback]

[Graph showing lithography wavelength and feature size over time, with key milestones such as 365nm, 248nm, 193nm, 130nm, 90nm, 65nm, and 13nm EUV.]

[Courtesy Intel]
AI / Cu / W wires
Planar CMOS
LE
Patterning
Transistors
Complexity
Interconnect
2005 2010 2015 2020 2025
[Courtesy ARM]
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[Courtesy ARM]
Solution: Layout Regularity

- Extreme lithography friendly
- Example: NAND cell [Liebmann et al. SPIE’13]
- How about the coming 10nm or even 7nm?

(a) 90nm

(b) 22nm
More about Middle-Of-Line (MOL)

- Local Interconnect (LI) or Intermediate Metallization (IM)
- 2 layers: CA (drain ↔ source), CB (via0 ↔ polys)
- Improve intra-cell routability
- Regular; SADP friendly [Luk-Pat et al, SPIE’13]

New standard cell structure is required
Pin Access Challenge

- Challenge in advanced tech nodes [Taghavi et al. ICCAD’10]
- Local detailed routing congestion
- Involve in standard cell design [Xu et al. ISPD’14]
- Both length & alignment of pins impact!

![Cell C1 and Cell C2](image)
Pin Access Challenge

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- Both length & alignment of pins impact!

- e.g.: C2 has better Pin Accessibility than C1
Pin Access Value

\[ p(i, j) = h_i + h_j - \alpha \cdot o(i, j) \]

- \( h_i \): track# of pin \( i \)
- \( o(i, j) \): overlapping track# between pins \( i \) and \( j \)

If \( \alpha = 0.6 \), then:

- \( p(a, c) = 3.8 \)
- \( p(a, d) = 5 \)
- \( p(c, d) = 4 \)
- \( p(a, b) = 5.8 \)
- \( p(b, d) = 6 \)

Total pin access value for whole standard cell:

\[ PA = \sum_{i=1}^{m} \sum_{j>i}^{m} p(i, j) \]
How Accurate of Pin Access Value?

- **Pin access combination #:** through expensive branch-and-bound search
- **Pin access value:** our simple model
- **Good fidelity!**
Problem Formulation

Input: original standard cell; design related parameters
Output: unidirectional (regular) cell layout w. MOL and SADP friendly
Objective: minimize the cell wirelength, and maximize the pin access value
More than Layout Migration

- ILP based [Fang et al. ASPDAC’04]
- LP based [Heng et al. ISPD’97][Salodkar et al. DAC’13]
- Longest-Path based [Tang et al. ICCAD’05]
More than Layout Migration

- ILP based [Fang et al. ASPDAC'04]
- LP based [Heng et al. ISPD'97][Salodkar et al. DAC'13]
- Longest-Path based [Tang et al. ICCAD’05]

Our work is **FIRST** cell synthesis for

- MOL, Regularity, Pin Access, SADP.
Overall Flow

Input 2D Cell Layout

Dummy Column Insertion

Grid Graph Construction

Cell Routing

Output 1D Cell Layout

Design Rules

ILP Based Cell Routing

Fast Cell Routing

Cell Layout

Input 2D Cell Layout
Dummy Column Insertion

- Some cross-couple gate connection structures
- Insert a dummy poly column to avoid illegal structure
Grid Graph Construction

- 3 routing areas: P tracks, M tracks, N tracks.
- 3 terminal types: P-terminals, M-terminals, N-terminals
Net Topo Enumeration

Example

▶ A net with 2 P-terminals and 1 N terminal
▶ Three possible routes for the net (assuming only one P, N, M track)
Overall Flow – ILP Based Cell Routing

1. Input 2D Cell Layout
2. Dummy Column Insertion
3. Grid Graph Construction
4. Cell Routing
5. ILP Based Cell Routing
6. Fast Cell Routing
7. Design Rules
8. Output 1D Cell Layout

Diagram:
- Input 2D Cell Layout
  - Dummy Column Insertion
  - Grid Graph Construction
  - Cell Routing
    - ILP Based Cell Routing
    - Fast Cell Routing
  - Output 1D Cell Layout
ILP Based Cell Routing

- Binary $x_i^p = 1 \iff$ net $i$ selects route topology $r_i^p$
- Metric 1: Pin Access $PA = \sum_{p_i, p_j \in N} \sum_{r_i \in R_i} \sum_{r_j \in R_j} p_{i,j}^{p,q} \cdot x_i^p \cdot x_j^q$
- Metric 2: Wire-Length $WL = \sum_{n_i \in N} \sum_{r_i \in R_i} w_i^p \cdot x_i^p$
ILP Based Cell Routing

- Binary $x_i^p = 1 \iff$ net $i$ selects route topology $r_i^p$
- Metric 1: Pin Access $PA = \sum_{p_i,p_j \in N} \sum_{r_i \in R_i} \sum_{r_j \in R_j} p_{i,j}^p \cdot x_i^p \cdot x_j^q$
- Metric 2: Wire-Length $WL = \sum_{n_i \in N} \sum_{r_i \in R_i} w_i^p \cdot x_i^p$

Mathematical Formulation

$$\text{max} \quad \beta \cdot PA - WL$$
$$\text{s.t.} \quad \sum_{r_i^p \in R_i} x_i^p = 1 \quad \forall n_i \in N$$

$$x_i^p \in \{0, 1\} \quad \forall r_i^p \in R_i, \forall n_i \in N$$

$$x_i^p + x_j^q \leq 1, \quad \text{if } r_i^p, r_j^q \text{ conflict}$$
PA is NOT linear expression due to $x_i^p \cdot x_j^q$

new variable $x_{i,j}^{p,q}$ to replace $x_i^p \cdot x_j^q$

additional constraints:

$$
\begin{cases}
    x_{i,j}^{p,q} \geq x_i^p + x_j^q - 1 \\
    x_{i,j}^{p,q} \leq x_i^p, \quad x_{i,j}^{p,q} \leq x_j^q \\
    x_{i,j}^{p,q} \in \{0, 1\}
\end{cases}
$$
PA is NOT linear expression due to $x_i^p \cdot x_j^q$

new variable $x_{i,j}^{p,q}$ to replace $x_i^p \cdot x_j^q$

additional constraints:

\[
\begin{align*}
    x_{i,j}^{p,q} & \geq x_i^p + x_j^q - 1 \\
    x_{i,j}^{p,q} & \leq x_i^p, \quad x_{i,j}^{p,q} \leq x_j^q \\
    x_{i,j}^{p,q} & \in \{0, 1\}
\end{align*}
\]

Transform to 0-1 ILP Formulation

Optimal but suffers from runtime overhead
Overall Flow – Fast Cell Routing

1. Input 2D Cell Layout
2. Dummy Column Insertion
3. Grid Graph Construction
4. Cell Routing
5. ILP Based Cell Routing
6. Fast Cell Routing
7. Output 1D Cell Layout
8. Design Rules
Step 1: M Track Assignment

- Limited M-track resource
- **Block points**: poly grids blocked due to connection of Metal-2 wires

> net $i \in BLK(j)$, if will add block on column $j$
> otherwise, $i \in NET(j)$
Step 1: M Track Assignment (cont.)

LP Formulation

\[
\max \sum_i b_i \cdot x_i \\
\text{s.t.} \sum_{i \in NET(j)} x_i \leq T_m - |BLK(j)| \quad \forall \text{column } j
\]

- \( b_i \): benefit to assign net \( i \) into M-track
Step 2: P/N Track Assignment

2-SAT Formulation

\[ \text{FALSE} = \neg x_i \cdot x_j \iff \text{TRUE} = x_i + \neg x_j \]

- Optimally solved through strongly connected component
- Linear runtime
Step 3: I/O Pin Extension

\[
\max \sum_{i=1}^{m} (l_i^0 - l_i) + (r_i - r_i^0)
\]

s.t. \[c_L \leq l_i \leq l_i^0 \quad \forall w_i \in PW\]

\[r_i^0 \leq r_i \leq c_R \quad \forall w_i \in PW\]

\[r_i - l_i \geq l_0 \quad \forall w_i \in PW\]

\[l_j - r_i \geq l_1 \quad \forall w_i, w_j \in \text{same track}\]

- LP formulation, Unimodular
- Dual to Min-Cost Flow

Diagram showing the process of I/O pin extension.
Step 4: Finish All Connections

- Vertical connections through CA
- Insert poly
Experimental Setup

Parameters

\[ p(i,j) = h_i + h_j - \alpha \cdot o(i,j) \]
\[ \max \beta \cdot PA - WL \]

\[ \Rightarrow \alpha = 0.6 \]
\[ \Rightarrow \beta = 0.02 \]

- C++; Linux machine with 3.3GHz CPU
- Input: Nangate 45nm standard cell library
- Target at 10nm technology node with SADP process.
- ILP/LP Solver: GUROBI
Results – Case 1

- **Input** CLKGATE_X1
Results – Case 1

- **Input** CLKGATE\_X1

- **Output** [Fast Routing]

(a) 9-track

(b) 10-track
Results – Case 2

- Input SDFFRS

(a) 9-track
(b) 10-track
Results – Case 2

- **Input** SDFFRS
- **Output** [Fast Routing]

(a) 9-track

(b) 10-track
Results – 9 V.S. 10 Tracks

On **Wire-Length (WL)** [ILP Routing]

- **Similar** total WL
- **Different** on M-2 WL → impact routing resource
On Pin Access Value (PA) [ILP Routing]

- 10-track introduces 8% pin-access value against 9-track
- Trade-off: cell height \textit{v.s.} pin accessibility
Results – ILP V.S. Fast Cell Routing

Comparison on **Wire-Length (WL)**

- Fast cell routing: 0.7% Better total WL
Results – ILP V.S. Fast Cell Routing (cont.)

Comparison on Pin-Access Value (PA)

(a) 9-Track

(b) 10-Track

Fast cell routing: 2% Worse PA
Results – ILP V.S. Fast Cell Routing (cont.)

Comparison on **CPU Runtime**

(a) 9-Track

(b) 10-Track

- Fast cell routing: $10,000 \times$ speed-up
Conclusion and Future Work

- **First** cell synthesis toward better:
  - MOL structure
  - Regularity
  - Pin access
  - SADP friendly
- ILP cell routing: **optimal**
- Fast cell routing: **trade-off**

Future Work

- Flexibility to other **lithography** techniques
- Transistor **placement**
- Standard Cell **Characterization**
Thank You!

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