

3D-Flow: Flow-based Standard Cell Legalization for 3D ICs

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Introduction

- Placement legalization is a critical step in the physical design flow.
- An ideal legalization algorithm removes all overlap of instances while preserving the quality of the given placement.
- 3D integrated circuits (3D ICs) have emerged as a viable solution to extend Moore's Law.



Legalization as a Minimum-Cost Flow Problem

• Based on the flow network G(V, E), we can model the legalization as an assignment problem.

$$\min \sum_{(u,v)\in E} \sum_{c\in\Gamma(u)} \operatorname{cost}_{u,v,c} a_{u,v,c}$$
s.t.
$$\sum_{u\in V} \sum_{c\in\Gamma(v)} w_c a_{v,u,c} - \sum_{u\in V} \sum_{c\in\Gamma(u)} w_c a_{u,v,c} \ge \sup(v), \quad \forall v \in S$$

$$\sum_{u\in V} \sum_{c\in\Gamma(u)} w_c a_{u,v,c} - \sum_{u\in V} \sum_{c\in\Gamma(v)} w_c a_{v,u,c} \le \operatorname{dem}(v), \quad \forall v \in T \quad (3)$$

$$\sum_{u\in V} \sum_{c\in\Gamma(u)} w_c a_{u,v,c} - \sum_{u\in V} \sum_{c\in\Gamma(v)} w_c a_{v,u,c} = 0, \quad \forall v \in R$$

$$a_{u,v,c} \in \{0,1\}, \quad \forall (u,v) \in E, \forall c \in \Gamma(u),$$

where $a_{u,v,c} = 1$ indicates cell $c \in \Gamma(u)$ is moved from bin u to v.

Experimental Results

Table 1. Comparison on the legalization results of our 3D-Flow legalizer with existing SOTA legalizers for ICCAD 2022 benchmarks [6]. **RT** (s) stands for the total runtime including file IO. The average displacement and maximum displacement are normalized by the row height.

ICCAD 2022	Tetris [4]			Abacus [7]			BonnPlaceLegal [1]			Ours		
	Avg. Disp.	Max. Disp.	RT	Avg. Disp.	Max. Disp.	RT	Avg. Disp.	Max. Disp.	RT	Avg. Disp.	Max. Disp.	RT
case2	0.801	7.27	0.23	0.522	3.05	0.24	0.511	2.91	0.26	0.503	2.77	0.27
case2h	1.091	5.77	0.22	0.593	4.34	0.24	0.610	4.80	0.24	0.511	2.97	0.25
case3	0.929	13.40	1.15	0.705	5.81	1.35	0.727	6.13	2.70	0.660	4.53	1.54
case3h	1.162	8.30	1.19	0.938	9.47	1.44	0.986	7.95	6.28	0.750	4.61	1.73
case4	1.775	12.83	6.79	1.383	16.81	10.98	1.428	15.13	72.93	1.174	11.25	9.69
case4h	1.622	27.59	6.75	1.161	14.96	9.96	1.186	11.94	53.68	1.100	8.14	10.36
Average	1.613	2.31	0.76	1.125	1.54	0.95	1.153	1.43	3.34	1.000	1.00	1.00

Table 2. Comparison on the legalization results of our 3D-Flow legalizer with existing SOTA legalizers for ICCAD 2023 benchmarks [5]. **RT** (s) stands for the total runtime including file IO. The average displacement and maximum displacement are normalized by the row height.





Figure 1. Motivation for 3D-Flow legalizer. Global placement (a) is given for a 3D IC with two dies. (b) and (c) show legal placements, with red arrows indicating the cell displacement between global and legal placements. By moving two **blue**-colored cells (c) from the top to the bottom die, our 3D-Flow legalizer achieves reduced displacement.

Challenges:

- Greedy search methods fall in local optima.
- Formal optimization approaches are time-consuming.
- The vertical stacking in 3D ICs introduces new optimization opportunities.

3D Integrated Circuits

- 3D integration enables higher transistor density on the silicon and replaces the long 2D interconnects with shorter inter-die connections.
- There are mainly three types of 3D ICs: through-silicon-via (TSV)

The cost for such movement is calculated as:

 $D_{c}(v) = |x_{c} - x_{c}'| + |y_{c} - y_{c}'|, \quad \cos t_{u,v,c} = D_{c}(v) - D_{c}(u). \quad (4)$

• if w_c is constant for all cells, it is a minimum-cost flow problem.

• The successive shortest path algorithm for solving minimum-cost flow [3] is appropriate for our application.

3D-Flow Legalizer

Augmentation with Branch-and-Bound

- The traditional approach begins with a zero flow and iteratively employs Dijkstra's algorithm to identify the shortest paths between supply node *u* and demand node *v* in residual graph.
- We propose an enhanced algorithm that combines a modified BFS with branch-and-bound techniques to find the shortest augmenting path in 3D grid graph.



Figure 4. Path augmentation. (a) Candidate path with corresponding flow. (b) Cell movement with corresponding cost. A candidate path s - u - v for solving

ICCAD 2023	Tetris [4]			Abacus [7]			BonnPlaceLegal [1]			Ours		
		Max. Disp.	RT	Avg. Disp.	Max. Disp.	RT	Avg. Disp.	Max. Disp.	RT	Avg. Disp.	Max. Disp.	RT
case2	3.029	13.27	0.50	2.199	11.33	0.61	2.308	11.50	2.49	2.109	9.09	0.64
case2h1	3.609	50.28	0.57	2.509	35.28	0.68	2.668	36.85	4.80	2.433	27.03	0.74
case2h2	3.709	46.29	0.55	2.673	39.26	0.71	2.828	34.11	5.19	2.518	27.73	0.74
case3	3.612	195.31	3.07	2.475	136.25	4.52	2.615	131.96	59.83	2.442	70.82	4.46
case3h	3.041	141.31	2.89	2.266	119.31	4.21	2.370	109.11	69.99	2.204	99.05	5.74
case4	1.349	127.69	22.86	1.000	17.32	37.79	1.023	15.32	264.23	0.920	13.77	39.13
case4h	1.709	128.19	23.75	1.432	78.55	47.02	1.492	77.71	315.26	1.130	54.31	37.73
Average	1.461	2.97	0.69	1.076	1.40	1.00	1.127	1.34	8.89	1.000	1.00	1.00

- To validate our proposed 3D legalizer, we conducted experiments on ICCAD 2022 [6] and 2023 [5] contest benchmarks.
- We compared 3D-Flow legalizer with existing SOTA 2D legalizers including Tetris [4], Abacus [7], and BonnPlaceLegal [1].



Figure 7. HPWL increase (%) of global placement and legal placement for different methods. (a) ICCAD 2022 contest benchmarks. (b) ICCAD 2023 contest benchmarks.

based, monolithic, and face-to-face (F2F) bonding.



Figure 2. The typical types of 3D ICs. (a) F2F bonded 3D ICs enable heterogeneous technology integration without space crowding on the silicon layer. (b) TSVs occupy large silicon area, resulting in low integration density. (c) Monolithic 3D ICs require sequential fabrication with low yield.

the overflow in source bin s is shown in (a). At each step, the cells with minimal cost are selected to move. Since s and u belong to different dies, cell c_1 is moved completely. And u and v are horizontally adjacent, cell c_2 is moved partially to minimize displacement cost.



(a) Shortest Augmenting Path



(b) Eliminated Branch

Figure 5. Augmentation with branch and bound. (a) Augmenting path p_{best} with the smallest cost. (b) Eliminated branch with large cost. Moved cells are highlighted with red arrows indicating displacement. The **blue**-colored cell in (a) is from top die. The intermediate paths with large cost are stopped from being explored.

Legalization Within a Row

- After the flow-based legalization, cells are assigned to bins aligned with placement rows.
- We use the **PlaceRow** algorithm in Abacus [7] to remove the overlap between cells within bins.

Post-Optimization with Cycle-Canceling

Ablation study on die-to-die cell movement.





(a) w/o. D2D cell movement

(b) Our 3D-Flow Legalizer

Figure 8. Displacement visualization for the top die of **case3** in ICCAD 2023 contest benchmarks. (a) Without die-to-die (D2D) cell movement. (b)Using our 3D legalizer. The gray block represents the macro. The blue-colored cells in (b) are from the bottom die. Black lines indicate cell displacement.

Conclusion

- We propose the first 3D legalizer designed to minimize cell displacement for 3D ICs using network flow methods.
- By fully utilizing the vertical stacking, 3D-Flow legalizer finds legal positions for cells with minimal displacement in a global view.
- Our post-optimization with a cycle-canceling algorithm further reduces maximum displacement while preserving result quality.

Flow-based Legalization Formulation







planar

edegs

D2D

(1)

(2)

Figure 3. Flow network construction. (a) Cells are assigned to their nearest bins based on global placement. (b) Each bin is modeled as a vertex. Adjacent bins on the same die are connected by planar edges. And the bins on different dies with planar overlap are connected by die-to-die (D2D) edges.

- Each placement row is divided into uniform bins with a bin width denoted as $w_{\rm V}$.
- Adjacent bins on the same die are connected by planar edges, while bins on different dies with planar overlap are connected by die-to-die (D2D) edges.
- Movable cells C are assigned to their nearest dies and then to their nearest bins based on the global placement.
- Define the supply value for a bin v:

 $\sup(\mathbf{v}) = \max\{\mathbf{0}, \mathbf{w}_{\Gamma(\mathbf{v})} - \mathbf{w}_{\mathbf{v}}\},\$

similarly, define the demand value for a bin v:

 $\operatorname{dem}(v) = \max\{0, w_V - w_{\Gamma(V)}\},\$

- where $\Gamma(v)$ is the set of fractional cells assigned to bin v, and $W_{\Gamma(V)} = \sum_{\gamma \in \Gamma(V)} W_{C_{\gamma}} \times \rho_{\gamma}.$
- Find an assignment of cells to bins such that no bin is overflowed while minimizing cell displacement.

• we propose a post-optimization technique inspired by the cycle-canceling algorithm [2] to minimize maximum displacement.



Figure 6. Post-optimization with cycle-canceling. (a) Negative cycle. (b) Reduced maximum displacement. The black dashed box indicates the initial position. Our algorithm only selects cells with displacement larger than the predifined threshold to move toward their initial positions. Our incremental legalization will reduce the maximum displacement while making minimal perturbation to other cells.

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