CENG3420 Homework 3

Due: Apr. 24, 2020

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Q1 (20%) For two direct-mapped cache design with a 32-bit address and a 16-bit address, the following bits of the address are used to access the cache (as in Table 1).

Table 1: Q1

	Tag	Index	Offset
a	31-10	9-5	4-0
b	15-10	9-4	3-0

1. What is the cache line size (in word)?
2. How many entries does the cache have?
3. What is the ratio between total bits required for such a cache implementation over the data storage bits?

Q2 (15%) Suppose there is a byte addressable computer with main memory size 256MB and a cache with 8 lines. Each cache line size is 64B. Assume **direct mapping** in the memory hierarchy. Calculate the following items.

1. How many bits do we need at least for the main memory address? The total cache size (in bits).
2. The line number corresponding to the main memory address 2333_{10}.

Q3 (10%) Consider a cache works at $5\times$ speed of main memory with hit rate of 75%. What is the speedup of the memory performance if such cache is used.

Q4 (15%) There is a computer that has 64MB byte-addressable main memory. Instructions and data are stored in separated caches, each of which has eight 64B cache lines. The data cache use **direct-mapping**. Now there are two programs in the following form.
`Program A:`

```
int a[64][64];
int sum_array1()
{
        int i,j,sum=0;
        for(i=0;i<64;i++)
                for(j=0;j<64;j++)
                        sum += a[i][j];
        return sum;
}
```

```
Program B:

int a[64][64];
int sum_array1()
{
        int i,j,sum=0;
        for(j=0;j<64;j++)
                for(i=0;i<64;i++)
                        sum += a[i][j];
        return sum;
}
```

Suppose `int` data is represented in 32-bit 2's complement and i,j,sum are stored in specific registers. Arrays are stored in row-major with the start address 320_{10} in the main memory. Answer the following questions.

1. What are the line numbers of the main memory blocks that contain `a[0][31]` and `a[2][2]` respectively? (Cache line number starts from 0)
2. What are the data cache hit rates of program A and B?

Q5 (15%) A byte-addressable computer uses 32-bit address to access main memory. Suppose the data cache has a size of 4KiB and works in **8-way set-associative**. Each block size is 16B.

1. How many bits in Tag, Index and Offset?
2. Calculate the total cache size (in bits) if it uses write back and LRU replacement.

Q6 (20%) There are several parameters that impact the overall size of the page table. Listed below are key page table parameters.

Table 2: Q6

Virtual Address Size	Page Size	Page Table Entry Size
32	16KiB	4bytes

1. Given the parameters shown above, calculate the total page table size for a system running 5 applications that utilize half of the memory available (half of the 32-bit virtual address space for each running).
2. A cache designer wants to increase the size of a virtually indexed, physically tagged cache. Given the page size shown above, is it possible to make a 64KiB direct-mapped cache, assuming 2 words per block?
3. How would the designer increase the data size of the cache?

Q7 (5%) Suppose a processor supports software configuration on handling cache write hits/miss strategy.

1. What strategy should be taken if:

(a) The processor mainly works on applications that require massive memory write operation and data access.

(b) The processor mainly works on applications that require massive memory write operation and data access but do not allow data inconsistency.

Explain why.

2. Exlain why virtual memory only uses **write-back** as its write strategy.