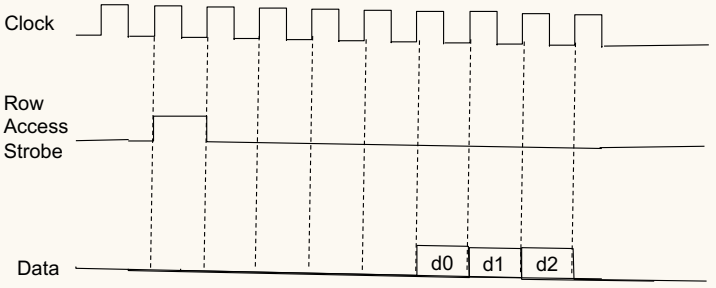
L08: Memory Organization

Name: _____

ID: _____

Question:

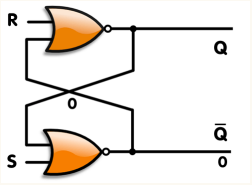
Suppose the clock rate is 500 MHz. What is the latency and what is the bandwidth, assuming that each data is 64 bits?



- 500 MHz = $2.0e^{-9}$ second

QUESTION:

Whats the Q value based on different R, S inputs?



Input		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

- R=S=1:
- S=0, R=1:
- S=1, R=0:
- R=S=0:

- R=S=0: latch holds current value
- S=0, R=1: set value to 0
- S=1, R=0:set value to 1
- R=S=1: not determined, not allowed

Question:

To transfer 8 bytes, what is the cycle# if just have TWO-module interleaved?

$$2 + 6 + 4 \times (\frac{n}{2} - 1) + 1,$$

where n is the byte# to transfer.