CENG3420 Homework 2

Due: Mar. 06, 2018

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DO NOT SUBMIT COMPRESSED ZIP or TARBALL.

Q1 (15%) The basic single-cycle MIPS implementation in Figure 1 can only implement some instructions. New instructions can be added to an existing Instruction Set Architecture. Following questions refer to the new instruction:

Instruction `LWI Rt, Rd(Rs)`

Interpretation `Reg[Rt] = Mem[Rd + Reg[Rs]]`

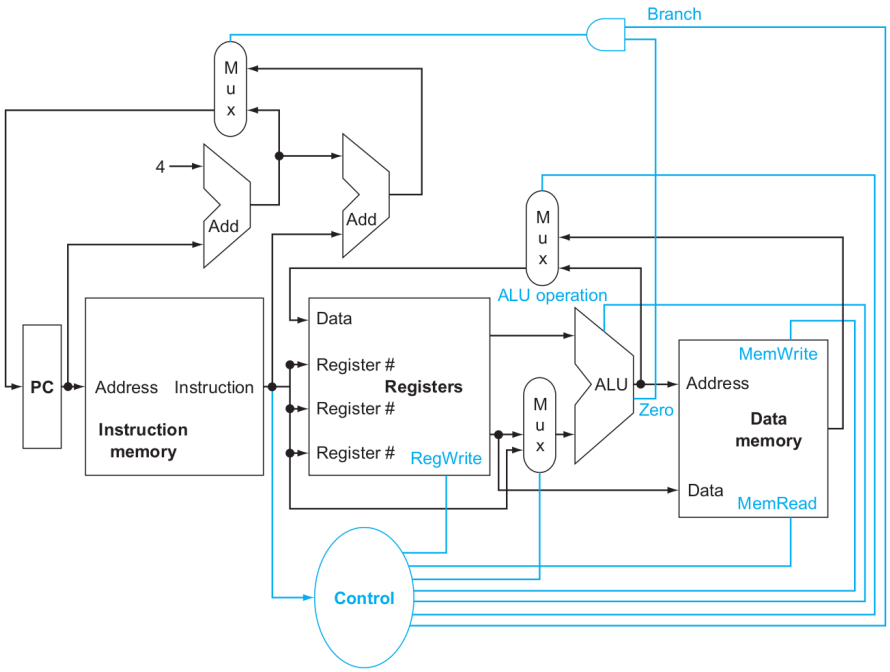

Figure 1: The basic implementation of the MIPS subset, including the necessary multiplexors and control lines.

1. Which existing blocks (if any) can be used for this instruction?
2. Which new functional blocks (if any) do we need for this instruction?
3. What new signals do we need (if any) from the control unit to support this instruction?

Q2 (15%) Following problems assume that logic blocks needed to implement a processor's datapath have the following latencies (Table 1):

1. If the only thing we need to do in a processor is fetch consecutive instructions (Figure 2), what would the cycle time be?

Table 1: Question 2

Item	I-Mem	Add	Mux	ALU	Regs	D-Mem	Sign-Extend	Shift-Left-2
Latency (ps)	200	70	20	90	90	250	15	10

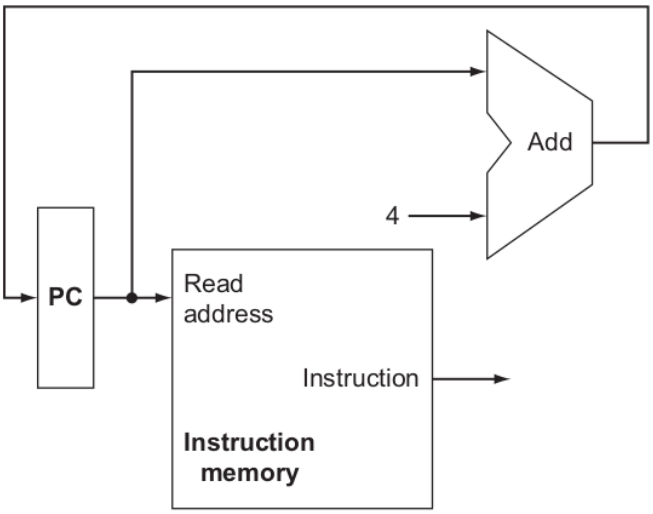

Figure 2: A portion of the datapath used for fetching instructions and incrementing the program counter.

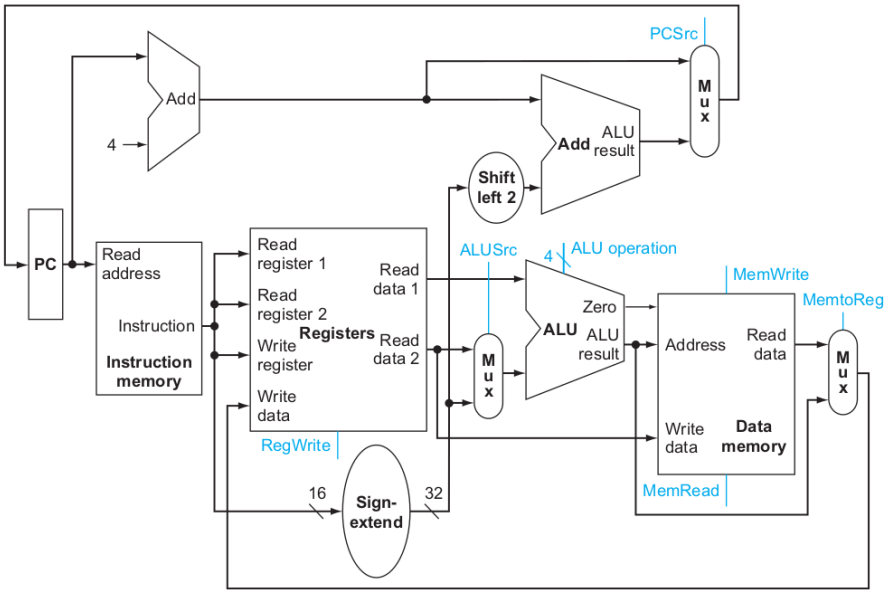

Figure 3: The simple datapath for the core MIPS architecture combines the elements required by different instruction classes.

2. Consider a datapath similar to the one in Figure 3, but for a processor that only has one type of instruction: unconditional PC-relative branch. What would the cycle time be for this datapath?
3. Repeat 2, but this time we need to support only conditional PC-relative branches.

Q3 (15%) Given the following specs of the datapath latencies:

Stages	IF	ID	EX	MEM	WB
Latencies (ps)	200	170	220	210	150

1. What is the clock cycle time in a pipelined and non-pipelined processor?
2. What is the total latency of an `LW` instruction in a pipelined and non-pipelined processor?
3. If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

Q4 (15%) Regarding the following instructions:

```
I1:  lw R1, 40(R2)
I2:  add R2, R3, R3
I3:  sw R2, 50(R1)
```

1. Indicate dependencies and their type.
2. Assume there is no forwarding in this pipelined processor. Add `NOP` instructions to eliminate hazards.
3. Assume there is full forwarding. Indicate hazards and add `NOP` instructions to eliminate them.

Q5 (10%) Assume it takes one clock to send address to DRAM memory and one clock to send data back. DRAM has 8 cycle latency for first byte, and 4 cycles for each of subsequent bytes in the block. To transfer a 8-byte block, calculate the cycle number if we need:

1. non-interleaving;
2. 2-module interleaving.

Q6 (**15%**) In this exercise we look at memory locality properties of matrix computation. The following code is written in C, where elements within the same row are stored contiguously.

```
for (J=0; J<8000; J++)
        for (I=0; I<8; I++)
                A[I][J]=B[J][I]+A[J][I];
```

1. How many 32-bit integers can be stored in a 16-byte cache line?
2. References to which variables exhibit temporal locality?
3. References to which variables exhibit spatial locality?

Q7 (10%) For a direct-mapped cache design with a 32-bit address, the following bits of the address are used to access the cache (as in Table 2).

1. What is the cache line size (in word)?

Table 2: Q7

	Tag	Index	Offset
a	31-10	9-5	4-0
b	31-12	11-6	5-0

2. What is the ratio between total bits required for such a cache implementation over the data storage bits?

Q8 (5%) Describe two cache replacement strategies.