**ARM Instruction set quick ref.**:[**www.arm.com**](http://www.arm.com)**,** [**http://simplemachines.it/doc/QRC0001H\_rvct\_v2.1\_arm.pdf**](http://simplemachines.it/doc/QRC0001H_rvct_v2.1_arm.pdf)

[**http://infocenter.arm.com/help/topic/com.arm.doc.qrc0001l/QRC0001\_UAL.pdf**](http://infocenter.arm.com/help/topic/com.arm.doc.qrc0001l/QRC0001_UAL.pdf)

|  |  |
| --- | --- |
| **Arithmetic** | ADD{condition}{S} Rd, Rn, <Operand> |
| ADC{condition}{S} Rd, Rn, <Operand> |
| SUB{condition}{S} Rd, Rn, <Operand> |
| SBC{condition}{S} Rd, Rn, <Operand> |
| RSB{condition}{S} Rd, Rn, <Operand> |
| RSC{condition}{S} Rd, Rn, <Operand> |
| MUL{condition}{S} Rd, Rm, Rs |
| MLA{condition}{S} Rd, Rm, Rs, Rn |
| UMULL{condition}{S} RdLo, RdHi, Rm, Rs |
| UMLAL{condition}{S} RdLo, RdHi, Rm, Rs |
| SMULL{condition}{S} RdLo, RdHi, Rm, Rs |
| SMLAL{condition}{S} RdLo, RdHi, Rm, Rs |
| **Move** | MOV{condition}{S} Rd, <Operand> |
| MVN{condition}{S} Rd, <Operand> |
| **Logical** | TST{condition} Rn, <Operand> |
| TEQ{condition} Rn, <Operand> |
| AND{condition}{S} Rd, Rn, <Operand> |
| EOR{condition}{S} Rd, Rn, <Operand> |
| ORR{condition}{S} Rd, Rn, <Operand> |
| BIC{condition}{S} Rd, Rn, <Operand> |
| **Compare** | CMP{condition} Rn, <Operand> |
| CMN{condition} Rn, <Operand> |
| **Branch** | B{condition} label |
| BL{condition} label |
| **Load / Store** | LDR{condition} Rd, <Addressing\_mode1> |
| STR{condition} Rd, <Addressing\_mode1> |
| **Stack** | LDM{condition}<Addressing\_mode2> Rn{!}, <register\_list> |
| STM{condition}<Addressing\_mode2> Rn{!}, <register\_list> |
| **Software Interrupt** | SWI{condition} #<immediate\_value> |

{S} means : Updates condition flags if S present

**Required fields**

|  |  |  |
| --- | --- | --- |
| **<Operand>** | | |
| Immediate value | #<immediate\_value> | |
| Register | Rm | |
| Logical shift left | Rm, LSL #<shift> | |
| Logical shift right | Rm, LSR #<shift> | |
| Arithmetic shift right | Rm, ASR #<shift> | |
| Rotate right | Rm, ROR #<shift> | |
| **<Addressing\_mode1>** | | |
| Zero offset | | [Rn] |
| Immediate offset | | [Rn, #+/-< immediate\_value>] |
| Register offset | | [Rn, +/-Rm] |
| Post-indexed Immediate offset | | [Rn], #+/-< immediate\_value> |
| Post-indexed Register offset | | [Rn], +/-Rm |
| Pre-indexed Immediate offset | | [Rn, #+/-< immediate\_value>]! |
| Pre-indexed Register offset | | [Rn, +/-Rm]! |
| **<Addressing\_mode2>** | | |
| Full Descending | | FD |
| Empty Descending | | ED |
| Full Ascending | | FA |
| Empty Ascending | | EA |

**Optional fields {condition}**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| EQ | Equal to zero (Z=1) |  | HI | Unsigned higher |
| NE | Not equal to zero (Z=0) |  | LS | Unsigned lower or same |
| MI | Negative |  | GE | Signed greater than or equal |
| PL | Positive or zero |  | LT | Signed less than |
| VS | Overflow |  | GT | Signed greater than |
| VC | No overflow |  | LE | Signed less than or equal |